bq24266 3-A, 30-V Standalone Single-Input, Single-Cell Switchmode Li-Ion Battery Charger

1 Features

- Charge Time Optimizer (Enhanced CC/CV Transition) for Faster Charging
- Integrated FETs for Up to 3A Charge Rate at 5% Accuracy and 93% Peak Efficiency
- Boost Capability to Supply 5V at 1A at IN for USB OTG Supply
- Integrated Power Path MOSFET and optional BGATE control to Maximize Battery Life and Instantly Startup From a Deeply Discharged Battery or No Battery
- 30V Input Rating with Over-Voltage Protection Supports 5V USB2.0/3.0 and 12V USB Power Delivery
- Small Solution Size In a 4mm x 4mm QFN-24 Package
- Safe and Accurate Battery Management Functions Programmed Using IUSB and /CE
  - Input Current Limit and V_{IN_DPM} Threshold
  - Thermal Regulation Protection for Input Current Control
  - Thermal Shutdown and Protection

2 Applications

- Handheld Scanner and Point of Sale Terminals
- Handheld Products
- Power Banks and External Battery Packs
- Small Power Tools
- Portable Media Players and Gaming

3 Description

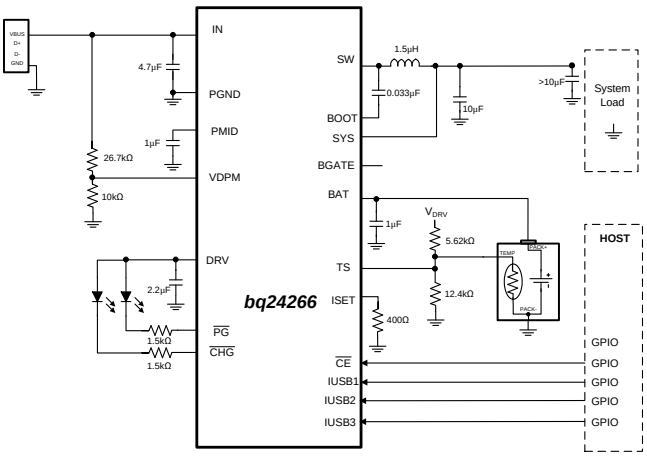
The bq24266 is highly integrated single cell Li-Ion battery charger and system power path management devices that supports operation from either a USB port or wall adapter supply. The power path feature allows the bq24266 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The power path also permits the battery to supplement the system current requirements when the adapter cannot. To support USB OTG applications, the bq24266 is configurable to boost the battery voltage to 5V and supply up to 1A at the input. The battery is charged with three phases: precharge, constant current and constant voltage. Thermal regulation prevents the die temperature from exceeding 125°C. Additionally, a JEITA compatible battery pack thermistor monitoring input (TS) is included to prevent the battery from charging outside of its safe temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24266	VQFN (24)	4.00mm × 4.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Revision History

Changes from Revision F (August 2015) to Revision G — **Page**

- Changed absolute maximum value for SYS, TS and I/O pins from 5.0 V to 5.5 V. ... 6
- Added $V_{IN} > V_{UVLO}$ test condition for $V_{BATUVLO}$. ... 10
- Changed image object for Figure 26 ... 28

Changes from Revision E (December 2014) to Revision F — **Page**

- Deleted devices bq24265 and bq24267 ... 1
- Changed bq2426x To: bq24266 throughout the datasheet ... 1
- Deleted Features: Host-controlled JEITA Compatible NTC Monitoring Input (bq24265) ... 1
- Deleted Features: Voltage-based, JEITA Compatible NTC Monitoring Input (bq24266) ... 1
- Changed text in the Description From: "The bq24265, bq24266, and bq24267 are.." To: "The bq24266 is.." ... 1
- Changed 1µF to 2.2µF on the DRV pin of the *Application Schematic* ... 1
- Deleted the *Device Comparison Table* ... 4
- Deleted the bq24265 pinout image ... 4
- Changed the DRV pin description From: "1µF of ceramic capacitance" To: "a 2.2uF, 10V, X5R or better capacitor" in the *Pin Functions* table ... 5
- Changed absolute maximum value for DRV pin from 5.0 V to 5.5 V. ... 6
- Moved the Stroage temperature to *Absolute Maximum Ratings*(1) ... 6
- Changed the *Handling Ratings* table To: ESD Ratings table ... 6
- Deleted references to BQ24265 and BQ24266 in V_{BATREG} of the *Electrical Characteristics* ... 8
- Deleted references to BQ24265 and BQ24266 in K_{ISET} of the *Electrical Characteristics* ... 8
- Deleted text from the *Overview section*: "The bq24265 allows a host to monitor a NTC thermistor and adjust the charge current and voltage using the $\overline{CE1}$ and $\overline{CE2}$ pins." and "The bq24267 features a TS input with HOT/COLD support only." ... 13
- Deleted text from the *Charge Profile* section: "using $\overline{CE1}$ and $\overline{CE2}$ (bq24265) or $\overline{CE}$ (bq24266/7)." ... 17
- Deleted text from the *Safety Timer in Charge Mode* section: " (bq24266/7) and when $\overline{CE1}$ and $\overline{CE2}$ (bq24265) are configured according to Table 2. ... 21

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- Changed the *External NTC Monitoring ($\overline{CE1}$, $\overline{CE2}$, and TS)* section To: *External NTC Monitoring (TS)* 21
- Deleted Table "$\overline{CE1}$, $\overline{CE2}$ Configurations" 21
- Deleted text from the *Application Information* section: "but can be used to evaluate the bq24265 or bq24267 as well. To configure the board to use the bq24265, the /CE1 and /CE2 pins are used to comply with JEITA per Table 2. 26
- Deleted the bq24265 Typical Application No External Discharge FET image 26

Changes from Revision D (October 2014) to Revision E **Page**

- Changed "Select 100kΩ for the bottom resistor" to "Select 10kΩ for the bottom resistor" in the *Input Voltage Based Dynamic Power Management (V_{IN}-DPM)* section..... 16

Changes from Revision C (October 2014) to Revision D **Page**

- Deleted text "TS faults are reported by the I^2C interface"; bq24266/7 TS pin description. 5
- Deleted text "or 2A (depending on the I^2C setting)" from *PWM Controller in Boost Mode* description. 24

Changes from Revision B (September 2014) to Revision C **Page**

- Changed the Test Conditions of $V_{SYSREG(LO)}$ From: $V_{BAT} < V_{MINSYS}$ To: $_{BAT} < V_{MINSYS}$, battery attached 7
- Deleted list item 3: $\overline{CE}$ pin = high from Battery Discharge FET (BGATE) 20

Changes from Revision A (August 2014) to Revision B **Page**

- Changed the text in the *Boost Mode Operation* section..... 24
- Added a NOTE to the *Application and Implementation* section 26

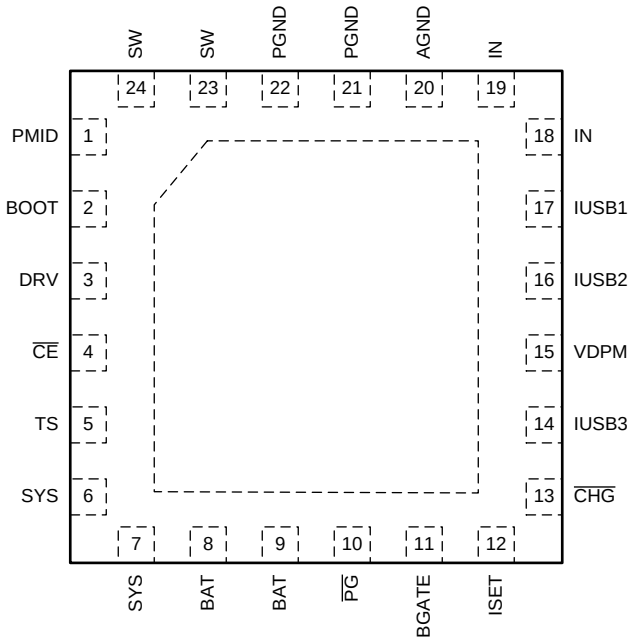
Changes from Original (June 2014) to Revision A **Page**

- Removed the Product Preview banner. 1

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5 Pin Configuration and Functions

RGE Package
24-Pin VQFN
Top View



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Pin Functions

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
AGND	20	–	Analog Ground. Connect to the thermal pad (for QFN only) and the ground plane of the circuit.
BAT	8, 9	I/O	Battery Connection. Connect to the positive pin of the battery. Bypass BAT to GND with at least 1µF of ceramic capacitance. See Application section for additional details.
BGATE	11	O	External Discharge MOSFET Gate Connection. BGATE drives an external P-Channel MOSFET to provide a very low resistance discharge path. Connect BGATE to the gate of the external MOSFET. BGATE is low during high impedance mode or when no input is connected. If no external FET is required, leave BGATE disconnected. Do not connect BGATE to GND.
BOOT	2	I	High Side MOSFET Gate Driver Supply. Connect 0.033µF of ceramic capacitance (voltage rating > 10V) from BOOT to SW to supply the gate drive for the high side MOSFET.
$\overline{CE}$	4	I	IC Charge Enable Input. Drive $\overline{CE}$ high to place the part to disable charge. Drive $\overline{CE}$ low for normal operation. $\overline{CE}$ is pulled low internally with 100kΩ.
$\overline{CHG}$	13	O	Charge Status Open Drain Output. $\overline{CHG}$ is pulled low when a charge cycle starts and remains low while charging. $\overline{CHG}$ is high impedance when the charging terminates and when when no supply exists.
DRV	3	O	Gate Drive Supply. DRV is the bias supply for the gate drive of the internal MOSFETs. Bypass DRV to PGND with at least a 2.2µF, 10V, X5R or better capacitor. DRV may be used to drive external loads up to 10mA. DRV is active whenever the input is connected and $V_{IN} > V_{UVLO}$ and $V_{IN} > (V_{BAT} + V_{SLP})$.
IN	18, 19	I	DC Input Power Supply. IN is connected to the external DC supply (AC adapter or USB port). Bypass IN to PGND with at least a 4.7µF of ceramic capacitance.
ISET	12	I	Charge Current Programming Input. Connect a resistor from ISET to GND to program the fast charge current. The charge current is programmable from 500mA to 3A.
IUSB1	17	I	USB Input Current Limit Programming Inputs. IUSB1, IUSB2 and IUSB3 program the input current limit for the USB input. USB2.0 and USB3.0 current limits are available for easy implementation of these standards. Table 1 shows the settings for these inputs.
IUSB2	16	I	
IUSB3	14	I	
$\overline{PG}$	10	O	Power Good Open Drain output. $\overline{PG}$ is pulled low wehn a valid supply is connected. A valud supply is between $V_{BAT}+V_{SLP}$ and V_{OVP}. The output is high impedance if the supply is not in this range.
PGND	21,22	–	Ground pin. Connect to the thermal pad (for QFN only) and the ground plane of the circuit.
PMID	1	I	High Side Bypass Connection. Connect at least 1µF of ceramic capacitance from PMID to PGND as close to the PMID and PGND pins as possible.
SW	23, 24	O	Inductor Connection. Connect to the switched side of the external inductor. The inductance must be between 1.5µH and 2.2µH.
SYS	6, 7	I	System Voltage Sense and Charger FET Connection. Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with at least 10µF of ceramic capacitance. The SYS rail must have at least 20µF of total capacitance for stable operation. See Application section for additional details.
TS	5	I	Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from DRV to GND. The NTC is connected from TS to GND. The TS function provides 4 thresholds for JEITA compatibility. Pull TS high to V_{DRV} to disable the TS function if unused. See the *NTC Monitor* section for more details on operation and selecting the resistor values.
VDPM	15	I	Input DPM Programming Input. Connect a resistor divider from IN to GND with VDPM connected to the center tap to program the Input Voltage based Dynamic Power Management (VIN_DPM) threshold. The input current is reduced to maintain the supply voltage at VIN_DPM. See the Input Voltage based Dynamid Power Management section for a detailed explanation.
Thermal PAD	–	–	There is an internal electrical connection between the exposed thermal pad and the PGND pin of the device. The thermal pad must be connected to the same potential as the PGND pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. PGND pin must be connected to ground at all times.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Pin Voltage (with respect to PGND)	IN	–1.3	30	V
	BOOT, PMID	–0.3	30	
	SW	–0.7	20	
	BAT	–0.3	5	
	DRV, BGATE, $\overline{CE}$, ISET, IUSB1, IUSB2, IUSB3, $\overline{PG}$, $\overline{CHG}$, SYS, TS	–0.3	5.5	
	AGND	-0.3	0.3	
BOOT to SW		–0.3	5	V
Output Current (Continuous)	SW		4.5	A
	SYS, BAT (charging/ discharging)		3.5	
Input Current (Continuous)			2.75	A
Output Sink Current	$\overline{CHG}$, $\overline{PG}$		10	mA
Operating free-air temperature		–40	85	°C
Junction temperature, T_J		–40	125	
Storage temperature, T_{stg}			300	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground pin unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	IN voltage range	4.2		13.5(1)	V
	IN operating voltage range	4.2		14	
I_{IN}	Input current, IN input			2.5	A
I_{SW}	Output Current from SW, DC			3	A
I_{BAT}, I_{SYS}	Charging			3	A
	Discharging, using internal battery FET			3	
T_J	Operating junction temperature range	0		125	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. A *tight* layout minimizes switching noise.

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6.4 Thermal Information

THERMAL METRIC(1)		bq24266 RGE (24 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.3	°C/W
$R_{JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Circuit of , $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+ V_{SLP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{IN}	Supply current for control	$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN}>V_{BAT}+V_{SLP}$ PWM switching		15		mA
		$V_{UVLO} < V_{IN} < V_{OVP}$ and $_{VIN}>V_{BAT}+V_{SLP}$ PWM NOT switching			6.65	
		0°C< T_J < 85°C, V_{IN} = 5V, High-Z Mode			250	µA
I_{BAT_HIZ}	Battery discharge current in High Impedance mode, (BAT, SW, SYS)	0°C< T_J < 85°C, V_{BAT} = 4.2 V, V_{IN} = 5V, SCL, SDA = 0V or 1.8V, High-Z Mode			15	µA
		0°C< T_J < 85°C, V_{BAT} = 4.2 V, V_{IN} = 0V, SCL, SDA = 0V or 1.8V			80	
POWER-PATH MANAGEMENT						
$V_{SYSREG(LO)}$	System Regulation Voltage	$V_{BAT} < V_{MINSYS}$, battery attached	V_{MINSYS} + 80mV	V_{MINSYS} + 100mV	V_{MINSYS} + 120mV	V
$V_{SYSREG(HI)}$	System Regulation Voltage	Battery FET turned off, no charging, V_{BAT} > 3.5V	V_{BATREG} +2.2%	V_{BATREG} +2.5%	V_{BATREG} +2.77%	V
V_{MINSYS}	Minimum System Voltage Regulation Threshold	$V_{BAT} + V_{DO(SYS_BAT)} < 3.5V$	3.44	3.5	3.55	V
$t_{DGL(MINSYS_CMP)}$	Deglitch time, VMINSYS comparator rising			8		ms
V_{BSUP1}	Enter supplement mode threshold	$V_{BAT} > V_{BUVLO}$		V_{BAT} – 20mV		V
V_{BSUP2}	Exit supplement mode threshold	$V_{BAT} > V_{BUVLO}$		V_{BAT} – 5mV		V
$I_{LIM(DISCH)}$	Current Limit, Discharge or Supplement Mode	$V_{LIM(BGATE)} = V_{BAT} – V_{SYS}$	4	6		A
$t_{DGL(SC1)}$	Deglitch Time, OUT Short Circuit during Discharge or Supplement Mode	Measured from I_{BAT} = 7A to FET off		250		µs
$t_{REC(SC1)}$	Recovery time, OUT Short Circuit during Discharge or Supplement Mode			2		s
	Battery Range for BGATE Operation		2.5		4.5	V

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Electrical Characteristics (continued)

Circuit of , $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+ V_{SLP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGER						
$R_{ON(BAT-SYS)}$	Internal battery charger MOSFET on-resistance	Measured from BAT to SYS, V_{BAT} = 4.2V, High-Z mode		32	47	mΩ
V_{BATREG}	Charge Voltage	T_J = 25°C	4.18	4.2	4.22	V
	Charge Voltage	T_J = 0°C to 85°C	4.17	4.2	4.23	V
	Charge Voltage	T_J = 0°C to 85°C, TS WARM	4.03	4.06	4.09	V
	Voltage Regulation Accuracy	T_J = 0°C to 125°C	-1.0%		1.0%	
I_{CHARGE}	Fast Charge Current Range	$V_{BATSHRT} \le V_{BAT} < V_{BAT(REG)}$	500		3000	mA
	Fast Charge Current Accuracy	500 mA ≤ I_{CHARGE} ≤ 1A	–10%		10%	
		I_{CHARGE} > 1000 mA	–5%		5%	
K_{ISET}	Programmable Fast Charge Current Factor	CE1=X, CE2=0, I_{CHARGE} > 1000 mA	1140	1200	1260	AΩ
		CE1=X, CE2=0, 500 mA ≤ I_{CHARGE} ≤ 1A	1080	1200	1320	AΩ
		TS COOL, I_{CHARGE} > 1000 mA	570	600	630	AΩ
		TS COOL, 500 mA ≤ I_{CHARGE} ≤ 1A	540	600	660	AΩ
$V_{BATSHRT}$	Battery short circuit threshold		2.9	3	3.1	V
$V_{BATSHRT_HYS}$	Hysteresis for $V_{BATSHRT}$	Battery voltage falling		100		mV
	Deglitch time for battery short to fastcharge transition	V_{BAT} rising or falling		1		ms
$I_{BATSHRT}$	Battery short circuit charge current	$V_{BAT} < V_{BATSHRT}$	33.5	.50	66.5	mA
I_{TERM}	Termination charge current	50mA ≤ I_{TERM} ≤ 300 mA		10		% of I_{CHARGE}
	Termination charge current accuracy	I_{TERM} ≤ 50 mA	–30%		30%	
		50 mA < $_{ITERM}$ < 200 mA	–15%		15%	
		I_{TERM} ≥ 200 mA	–15%		10%	
$t_{DGL(TERM)}$	Deglitch time for charge termination	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL}=100ns		32		ms
V_{RCH}	Recharge threshold voltage	Below V_{BATREG}	100	120	150	mV
$t_{DGL(RCH)}$	Deglitch time	V_{BAT} falling below V_{RCH}, t_{FALL}=100ns		32		ms
$V_{DET(SRC1)}$	Battery detection voltage threshold (TE = 1)	During current source (Turn $I_{BATSHRT\ off}$)		V_{RCH}		V
$V_{DET(SRC2)}$		During current source (Turn $I_{BATSHRT\ on}$)		V_{RCH} – 200mV		V
$V_{DET(SNK)}$		During current sink		$V_{BATSHRT}$		V
I_{DETECT}	Battery detection current before charge done (sink current)	Termination enabled (TE = 1)		7		mA
$t_{DETECT(SRC)}$	Battery detection time (sourcing current)	Termination enabled (TE = 1)		2		s
$t_{DETECT(SNK)}$	Battery detection time (sinking current)	Termination enabled (TE = 1)		250		ms

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Electrical Characteristics (continued)

Circuit of , $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+ V_{SLP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENT LIMITING							
I_{INLIM}	Input current limiting threshold	USB charge mode, V_{IN} = 5V, Current pulled from SW	I_{INLIM}=USB100	90	95	100	mA
			I_{INLIM}=USB500	450	475	500	
			I_{INLIM}=USB150	125	140	150	
			I_{INLIM}=USB900	800	850	900	
			I_{INLIM}=1.5A	1425	1500	1575	
			I_{INLIM}=2.5A	2225	2500	2825	
V_{IN_DPM}	Input based DPM threshold range	Charge mode, programmable via VDPM		4.2		11.6	V
V_{VDPM}	Feedback threshold			1.15	1.2	1.25	V
V_{DRV} BIAS REGULATOR							
V_{DRV}	Internal bias regulator voltage	V_{IN}>5V		4.3	4.8	5.3	V
I_{DRV}	DRV Output Current			0		10	mA
V_{DO_DRV}	DRV Dropout Voltage ($V_{IN\ –\ VDRV}$)	I_{IN} = 1A, V_{IN} = 4.2V, I_{DRV} = 10mA				450	mV
STATUS OUTPUT ($\overline{PG}$, $\overline{CHG}$)							
V_{OL}	Low-level output saturation voltage	I_O = 10 mA, sink current				0.4	V
I_{IH}	High-level leakage current	$V_{\overline{PG}} = V_{\overline{CHG}}$ = 5V				1	µA
INPUT PINS ($\overline{CE1}$, $\overline{CE2}$, IUSB1, IUSB2, IUSB3)							
V_{IL}	Input low threshold					0.4	V
V_{IH}	Input high threshold			1.4			V
$R_{PULLDOWN}$					100		kΩ

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Electrical Characteristics (continued)

Circuit of , $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+ V_{SLP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION						
V_{UVLO}	IC active threshold voltage	V_{IN} rising	3.2	3.3	3.4	V
V_{UVLO_HYS}	IC active hysteresis	V_{IN} falling from above V_{UVLO}		300		mV
$V_{BATUVLO}$	Battery Undervoltage Lockout threshold	V_{BAT} falling, $V_{IN}>V_{UVLO}$		2.4	2.6	V
V_{SLP}	Sleep-mode entry threshold, V_{IN}-V_{BAT}	2.0 V < V_{BAT} < V_{BATREG}, V_{IN} falling	0	40	120	mV
$t_{DGL(BAT)}$	Deglitch time, BAT above $V_{BATUVLO}$ before SYS starts to rise			1.2		ms
V_{SLP_HYS}	Sleep-mode exit hysteresis	V_{IN} rising above V_{SLP}	40	100	190	mV
$t_{DGL(VSLP)}$	Deglitch time for supply rising above V_{SLP}+V_{SLP_HYS}	Rising voltage, 2-mV over drive, t_{RISE}=100ns		30		ms
V_{OVP}	Input supply OVP threshold voltage	IN rising, 100mV hysteresis	13.6	14	14.4	V
$t_{DGL(BUCK_OVP)}$	Deglitch time, VIN OVP in Buck Mode	IN falling below V_{OVP}		30		ms
V_{BOVP}	Battery OVP threshold voltage	V_{BAT} threshold over V_{OREG} to turn off charger during charge	1.03 × V_{BATREG}	1.05 × V_{BATREG}	1.07 × V_{BATREG}	V
V_{BOVP_HYS}	V_{BOVP} hysteresis	Lower limit for V_{BAT} falling from above V_{BOVP}		1		% of V_{BATREG}
$t_{DGL(BOVP)}$	BOVP Deglitch	Battery entering/exiting BOVP		8		ms
$I_{CbCLIMIT}$	Cycle-by-cycle current limit	V_{SYS} shorted	4.1	4.5	4.9	A
T_{SHTDWN}	Thermal trip			150		°C
	Thermal hysteresis			10		°C
T_{REG}	Thermal regulation threshold	Input current begins to cut off		125		°C
	Safety Timer Time		29160	32400	35640	s
PWM						
R_{DSON_Q1}	Internal top MOSFET on-resistance	Measured from IN to SW		80	135	mΩ
R_{DSON_Q2}	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND		80	135	mΩ
f_{OSC}	Oscillator frequency		1.35	1.5	1.65	MHz
D_{MAX}	Maximum duty cycle			95%		
D_{MIN}	Minimum duty cycle		0%			
BATTERY-PACK NTC MONITOR						
V_{HOT}	High temperature threshold	V_{TS} falling, 2% V_{DRV} Hysteresis	27.3	30	32.6	%V_{DRV}
V_{WARM}	Warm temperature threshold	V_{TS} falling, 2% V_{DRV} Hysteresis	36.0	38.3	41.2	%V_{DRV}
V_{COOL}	Cool temperature threshold	V_{TS} rising, 2% V_{DRV} Hysteresis	54.7	56.4	58.1	%V_{DRV}
V_{COLD}	Low temperature threshold	V_{TS} rising, 2% V_{DRV} Hysteresis	58.2	60	61.8	%V_{DRV}
TSOFF	TS Disable threshold	V_{TS} rising, 4% V_{DRV} Hysteresis	80		85	%V_{DRV}
$t_{DGL(TS)}$	Deglitch time on TS change	Applies to V_{HOT}, V_{WARM}, V_{COOL} and V_{COLD}		50		ms

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Electrical Characteristics (continued)

Circuit of , $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT} + V_{SLP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OTG BOOST SUPPLY							
I_{QBAT_BOOST}	Quiescent current during boost mode (BAT pin)	3.3V<V_{BAT}<4.5V, no switching				100	µA
	Battery voltage range for specified boost operation	VBAT falling		3.3		4.5	V
V_{IN_BOOST}	Boost output voltage (to pin VBUS)	3.3V<V_{BAT}<4.5V over line and load		4.95	5.05	5.2	V
I_{BO}	Maximum output current for boost	3.3V<V_{BAT}<4.5V	BOOST_ILIM = 1	1000			mA
			BOOST_ILIM = 0	500			
I_{BLIMIT}	Cycle by cycle current limit for boost (measured at low-side FET)	3.3V<V_{BAT}<4.5V	BOOST_ILIM = 1		4		A
			BOOST_ILIM = 0		2		
$V_{BOOSTOVP}$	Over voltage protection threshold for boost (IN pin)	Signals fault and exits boost mode		5.8	6	6.2	V
$t_{DGL(BOOST_OVP)}$	Deglitch Time, VIN OVP in Boost Mode				170		µs
$V_{BURST(ENT)}$	Upper V_{IN} voltage threshold to enter burst mode (stop switching)			5.1	5.2	5.3	V
$V_{BURST(EXIT)}$	Lower V_{BUS} voltage threshold to exit burst mode (start switching)			4.9	5	5.1	V

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency		1.35	1.5	1.65	Mhz
D_{MAX}	Maximum duty cycle			95%		
D_{MIN}	Minimum duty cycle		0%			

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6.7 Typical Characteristics

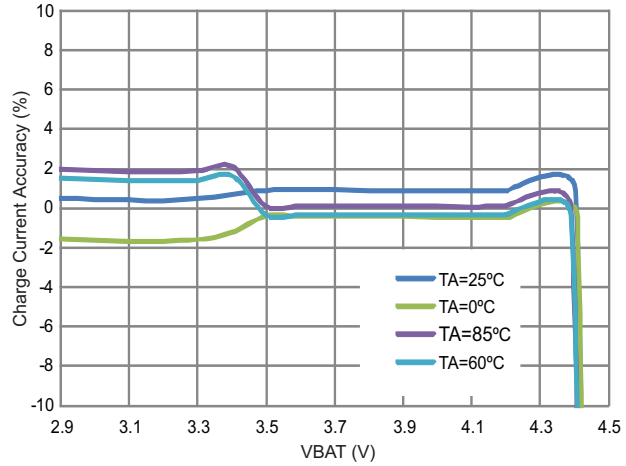


Figure 1. Charge Current vs Battery Voltage

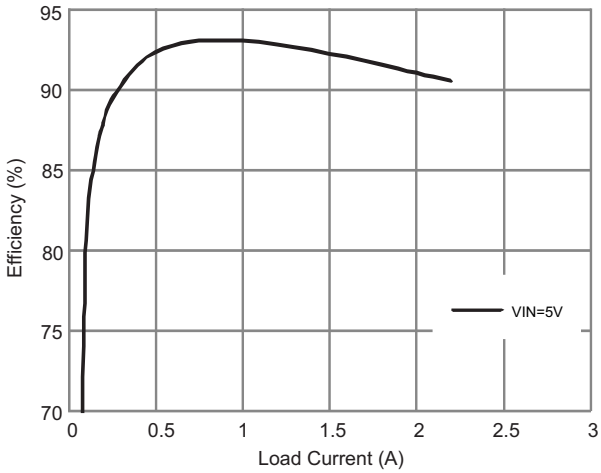


Figure 2. Efficiency vs Output Current

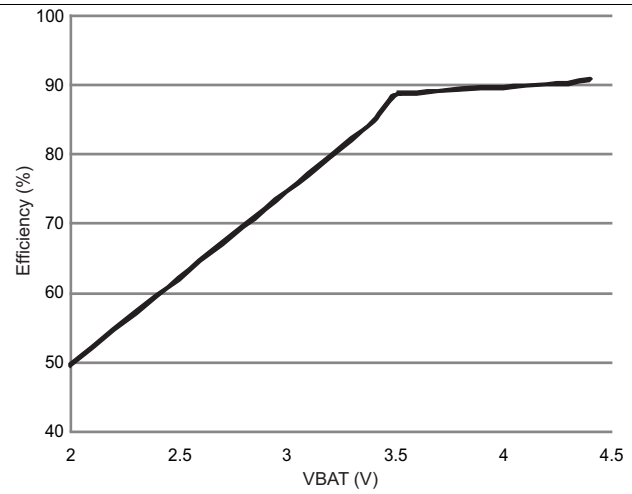


Figure 3. Efficiency vs Battery Voltage

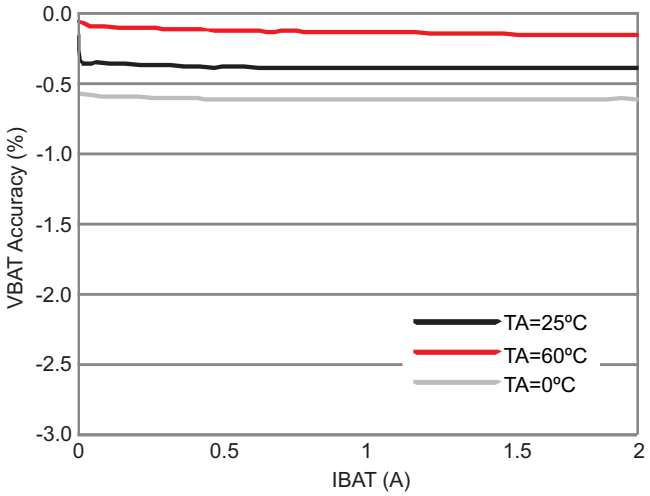


Figure 4. VBAT Accuracy vs IBAT – 4.2 VBAT

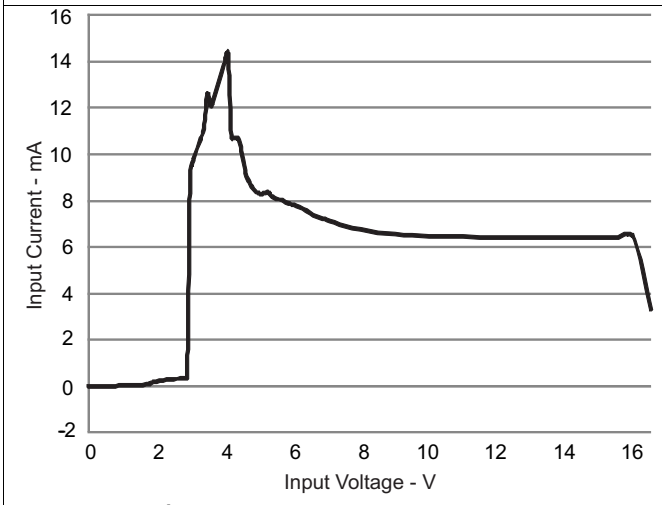


Figure 5. Input IQ - No Battery, No System

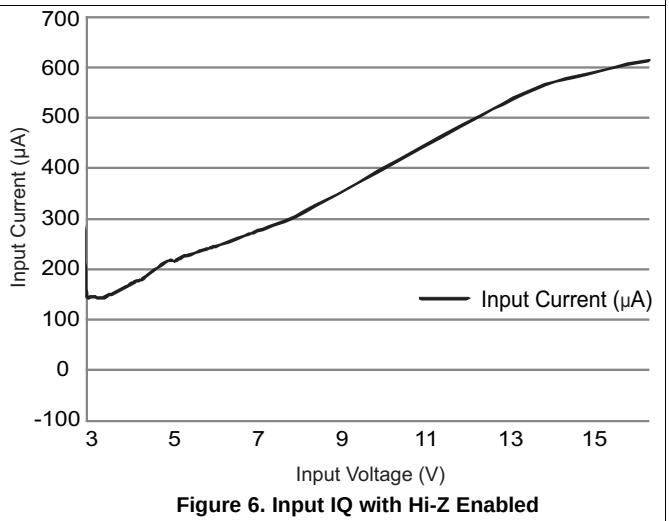


Figure 6. Input IQ with Hi-Z Enabled

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7 Detailed Description

7.1 Overview

The bq24266 is a highly integrated single cell Li-Ion battery charger and system power path management devices targeted for space-limited, portable applications with high capacity batteries. The single cell charger has a single input that supports operation from either a USB port or wall adapter supply for a versatile solution.

The power path management feature allows the bq24266 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit or the adapter cannot support the required load, causing the adapter voltage to fall (V_{IN_DPM}). This allows for proper charge termination and timer operation. The system voltage is regulated to the battery voltage but will not drop below 3.5V (V_{MINSYS}). This minimum system voltage support enables the system to run with a defective or absent battery pack and enables instant system turn-on even with a totally discharged battery or no battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. The power-path feature coupled with V_{IN}-DPM, enables the use of many adapters with no hardware change. The charge parameters are programmable using the ISET pin. To support USB OTG applications, the bq24266 is configurable to boost the battery voltage to 5V at the input. In this mode, the bq24266 supplies up to 1A and operates with battery voltages down to 3.3V.

The battery is charged using a standard Li-Ion charge profile with three phases: precharge, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the input current to prevent the junction temperature from rising above 125°C. With the bq24266 a voltage-based, JEITA compatible battery pack thermistor monitoring input (TS) is included that monitors battery temperature and automatically changes charge parameters to prevent the battery from charging outside of its safe temperature range.

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7.2 Functional Block Diagram

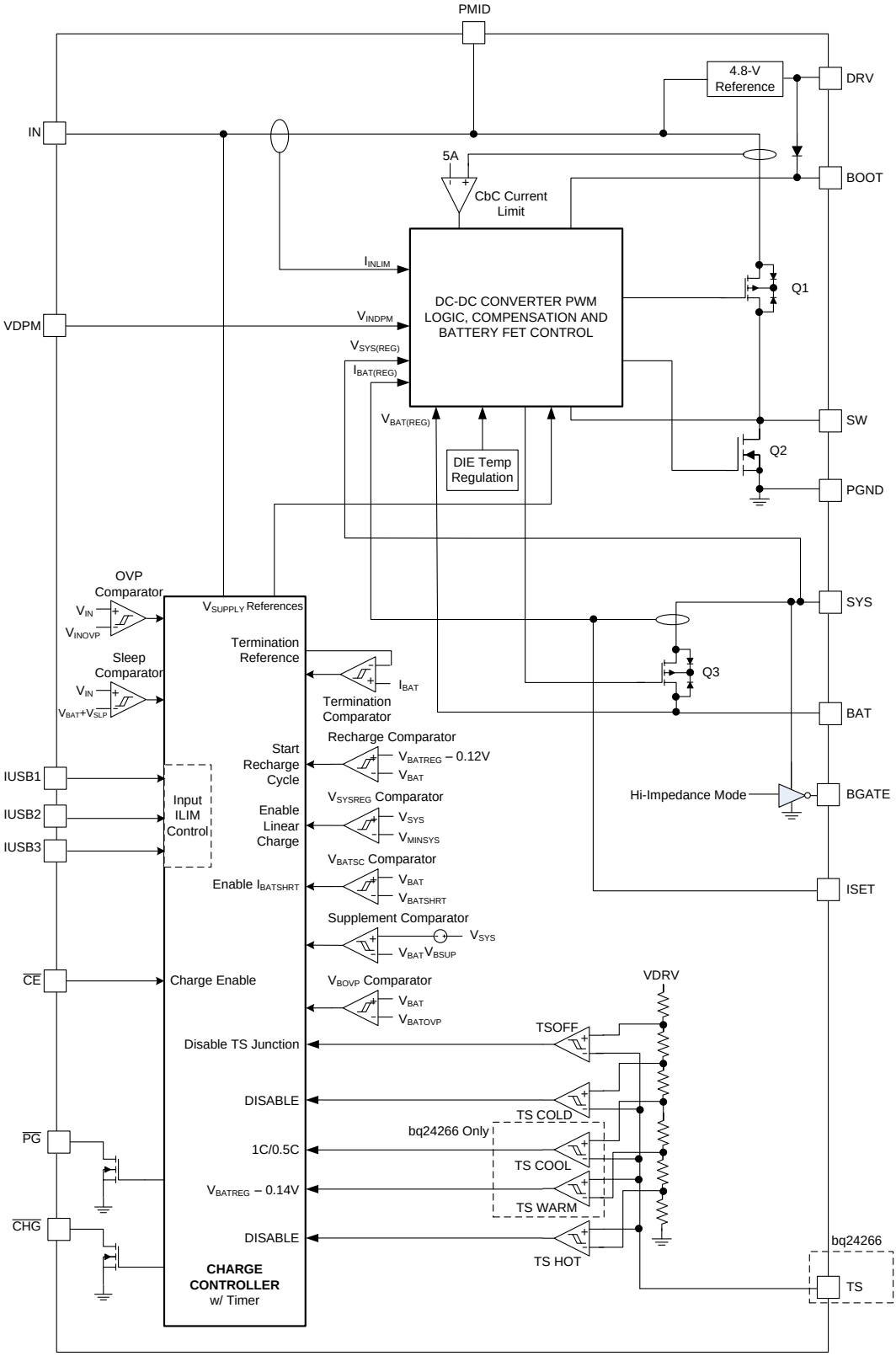


Figure 7. Block Diagram in Charging Mode

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Functional Block Diagram (continued)

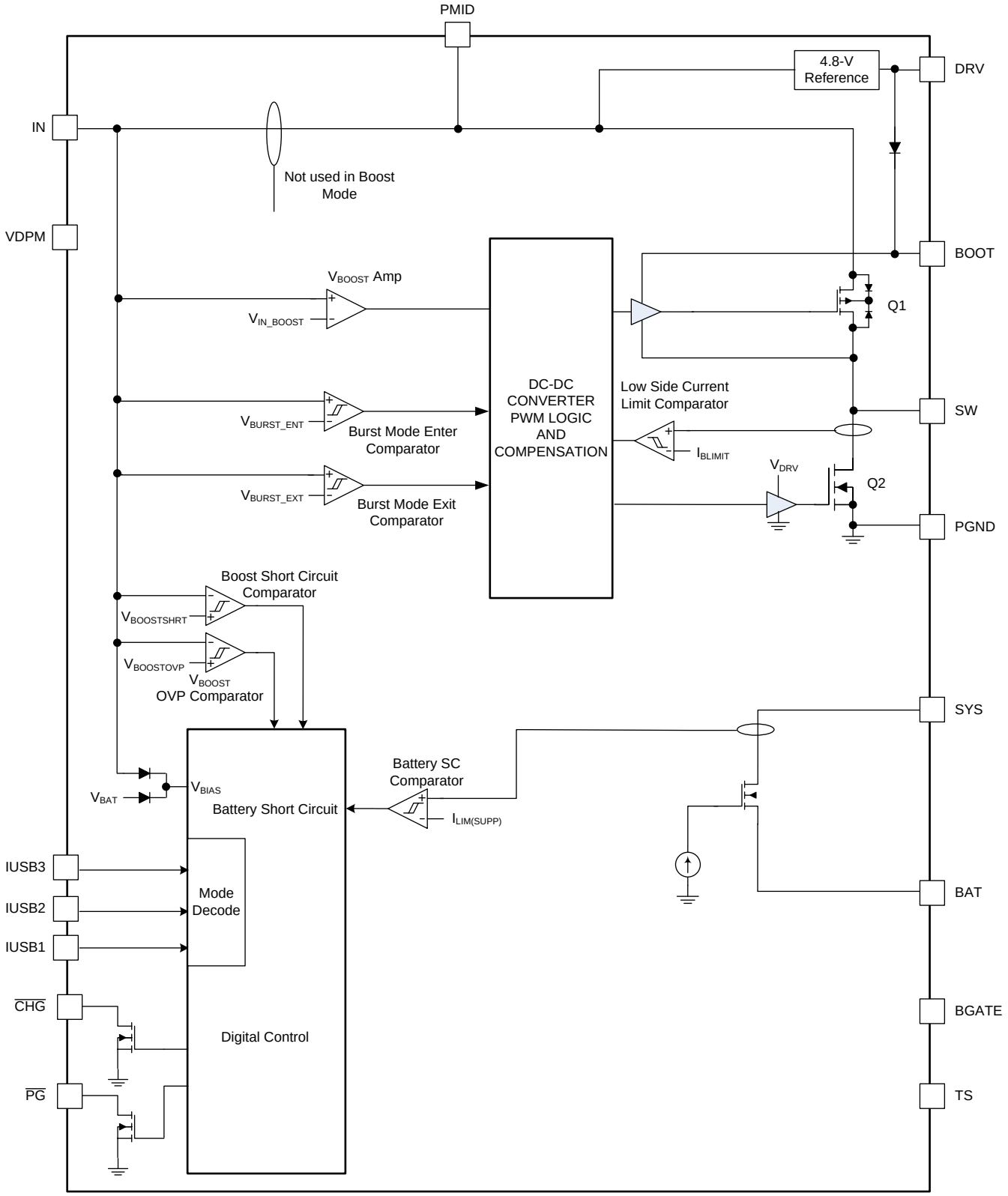


Figure 8. Block Diagram in Boost Mode

7.3 Feature Description

The bq24266 is a highly integrated single cell Li-Ion battery charger and system power path management devices that supports operation from either a USB port or wall adapter supply. The power path feature allows the bq24266 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The power path also permits the battery to supplement the system current requirements when the adapter cannot. Many features are programmable using dedicated pins. To support USB OTG applications, the bq24266 is configurable to boost the battery voltage to 5V and supply up to 1A at the input. The battery is charged with three phases: precharge, constant current and constant voltage. Thermal regulation prevents the die temperature from exceeding 125°C. With the bq24266, a JEITA compatible battery pack thermistor monitoring input (TS) is included to prevent the battery from charging outside of its safe temperature range.

7.4 Device Functional Modes

7.4.1 High Impedance Mode

High Impedance mode (Hi-Z mode) is the low quiescent current state for the bq24266. During Hi-Z mode, the buck converter is off, and the battery FET and BGATE are on. SYS is powered by BAT. The bq24266 is in Hi-Z mode when $V_{IN} < V_{UVLO}$ or the IUSB1, IUSB2, and IUSB3 pins are all driven high. Hi-Z mode resets the safety timer. When exiting Hi-Z mode, charging resumes in approximately 110ms.

7.4.2 Battery Only Connected

When the battery is connected with no input source, the battery FET turns on, connecting BAT and SYS, after the battery voltage rises above $V_{BATUVLO}$ and the deglitch time, $t_{DGL(BAT)}$. In this mode, the current is not regulated; however, there is a short circuit current limit. If the short circuit limit ($I_{LIM(DISCHG)}$) is reached for the deglitch time ($t_{DGL(SC)}$), the battery FET is turned off for the recovery time ($t_{REC(SC)}$). After the recovery time, the battery FET is turned on to test and see if the short has been removed. If it has not, the FET turns off and the process repeats until the short is removed. This process protects the internal FET from over current. If an external FET is used for discharge, the body diode prevents the load on SYS from being disconnected from the battery and $t_{DGL(BAT)}$ is not applicable.

7.4.3 Input Connected

7.4.3.1 Input Voltage Protection in Charge Mode

7.4.3.1.1 Sleep Mode

The bq24266 enters the low-power sleep mode if the voltage on V_{IN} falls below sleep-mode entry threshold, $V_{BAT}+V_{SLP}$, and V_{IN} is higher than the undervoltage lockout threshold, V_{UVLO}. In sleep mode, the input is isolated from the battery. This feature prevents draining the battery during the absence of V_{IN}. When $V_{IN} < V_{BAT}+ V_{SLP}$, the bq24266 turns off the PWM converter and turns the battery FET and BGATE on. Once $V_{IN} > V_{BAT}+ V_{SLP}$, the device initiates a new charge cycle.

7.4.3.1.2 Input Voltage Based Dynamic Power Management (V_{IN}-DPM)

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage deceases. Also, at higher currents, large input line impedances may cause the voltage at the device to droop. Once the supply drops to V_{IN_DPM} (default 4.2V), the charge current limit is reduced to prevent the further drop of the supply. When the IC enters this mode, the charge current is lower than the set value. This feature ensures IC compatibility with adapters with different current capabilities without a hardware change. Figure 9 shows the V_{IN}-DPM behavior to a current limited source. In this figure the input source has a 2A current limit and the device is charging at 1A. A 2.5A load transient then occurs on V_{SYS} causing the adapter to hit its current limit and collapse, while V_{SYS} goes from $V_{SYSREG(LO)}$ to V_{MINSYS}. The safety timer is extended while V_{IN}-DPM is active. Additionally, termination is disabled.

The V_{INDPM} threshold for the adapter modes (1.5A and 2.5A) is set using a resistor divider with VDPM connected to the center tap. Select 10kΩ for the bottom resistor. The top resistor is selected using equation Equation 1.

Where V_{IN_DPM} is the desired V_{IN_DPM} threshold and VDPM is the regulation threshold at the pin specified in the Electrical Characteristics table.

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Device Functional Modes (continued)

$$RTOP = 10k\Omega \times \frac{VIN_DPM\text{-}VDPM}{VDPM} \quad (1)$$

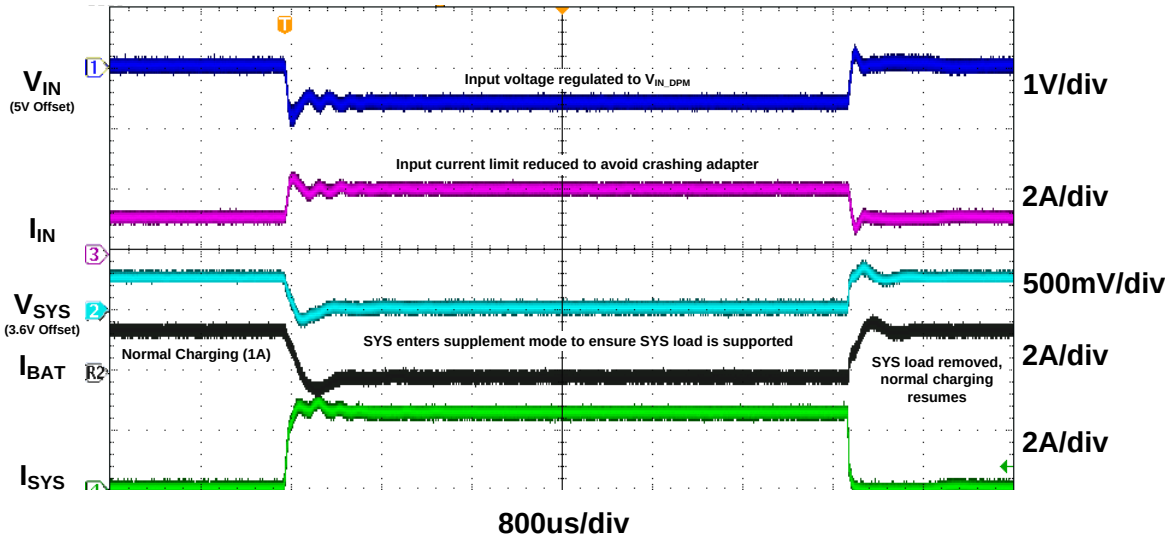


Figure 9. bq24266 V_{IN}-DPM

7.4.3.1.3 Input Overvoltage Protection

The built-in input overvoltage protection protects the bq24266 and downstream components connected to SYS and/or BAT against damage from overvoltage on the input supply (Voltage from V_{IN} to PGND). When $V_{IN} > V_{OVP}$, the bq24266 turns off the PWM converter immediately. After the deglitch time $t_{DGL(BUCK_OVP)}$, an OVP fault is determined to exist. During the OVP fault the bq24266 turns the battery FET and BGATE on. Once the OVP fault is removed, the device returns to normal operation.

The OVP threshold is 14V for operation from standard adapters and from 12V sources.

7.4.3.2 Charge Profile

When a valid input source is connected ($V_{IN}>V_{UVLO}$ and $V_{BAT}+V_{SLP}<V_{IN}<V_{OVP}$), charging is enabled.

The charge current, I_{CHARGE}, is set using the ISET pin by connecting a resistor form ISET to GND. The current is programmable from 500mA to 3A using Equation 2, where I_{CHARGE} is in Amperes, and K_{ISET} is the value specified in the *Electrical Characteristics* table.

$$R_{CHARGE} = \frac{K_{ISET}}{R_{ISET}} \quad (2)$$

The bq24266 supports a precision Li-Ion or Li-Polymer charging system for single-cell applications. Charging is done through the internal battery MOSFET. There are 6 loops that influence the charge current; constant current loop (CC), constant voltage loop (CV), thermal regulation loop, minimum system voltage loop (MINSYS), input current limit and V_{IN}-DPM. During the charging process, all six loops are enabled and the one that is dominant takes control. The minimum system output feature regulates the system voltage to $V_{SYSREG(LO)}$, so that startup is enabled even for a missing or deeply discharged battery. Figure 10 shows a typical charge profile including the minimum system output voltage feature.

Device Functional Modes (continued)

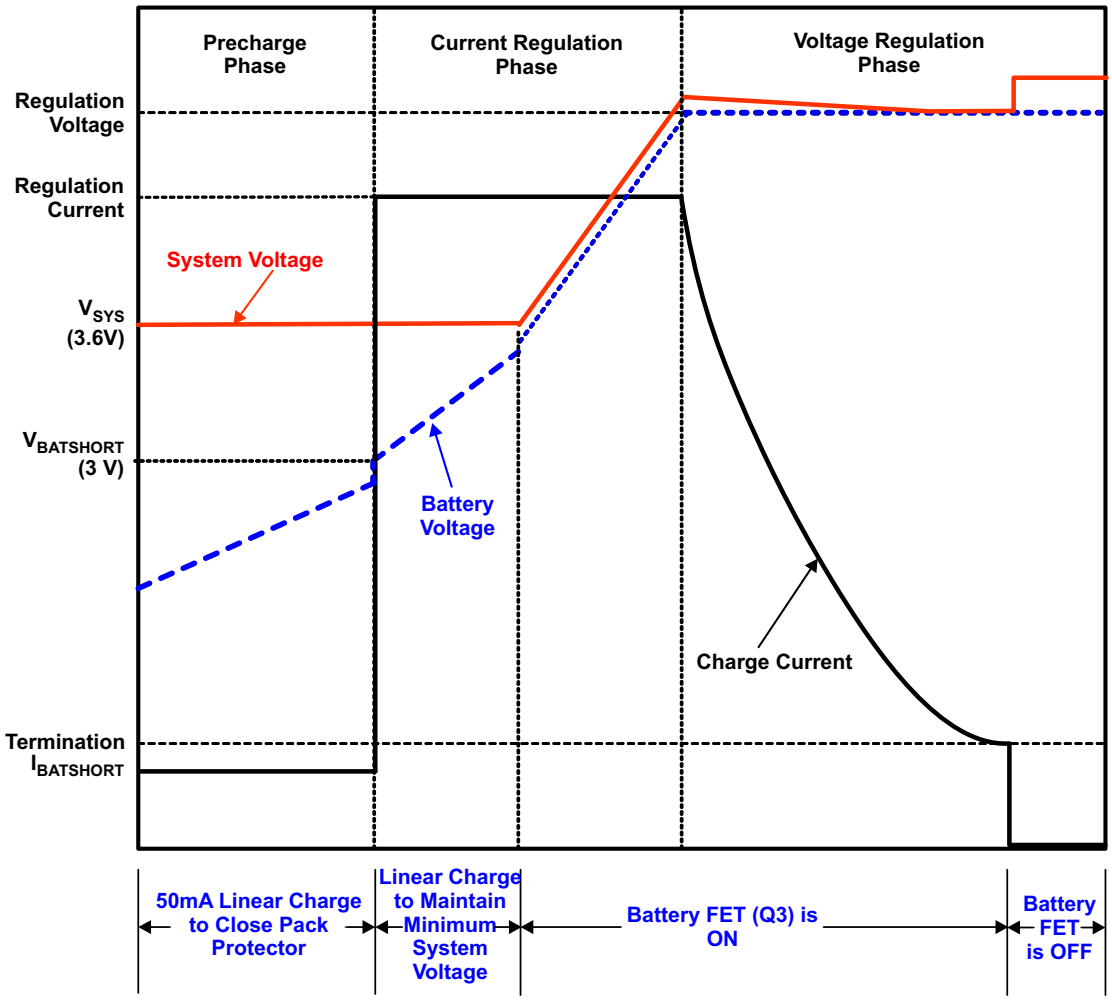


Figure 10. Typical Charging Profile of bq24266

7.4.4 Battery Charging Process

When the battery is deeply discharged or shorted, the bq24266 applies a $I_{BATSHRT}$ current to close the battery protector switch and bring the battery voltage up to acceptable charging levels. During this time, the battery FET is off and the system output is regulated to $V_{SYSREG(LO)}$. Once the battery rises above $V_{BATSHRT}$, the charge current is regulated to the value set by ISET. The battery FET is linearly regulated to maintain the system voltage at $V_{SYSREG(LO)}$. Under normal conditions, the time spent in this region is a very short percentage of the total charging time, so the linear regulation of the charge current does not affect the overall charging efficiency for very long. If the die temperature does heat up, the thermal regulation loop reduces the input current to maintain a die temperature at 125°C. If the current limit for the SYS output is reached (limited by the input current limit, V_{IN}-DPM, or 100% duty cycle), the SYS output drops to the V_{MINSYS} output voltage. When this happens, the charge current is reduced to ensure the system is supplied with all the current that is needed while maintaining the minimum system voltage. If the charge current is reduced to 0mA, pulling further current from SYS causes the output to fall to the battery voltage and enter supplement mode (see the “Dynamic Power Path Management” section for more details).

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Device Functional Modes (continued)

Once the battery is charged enough that the system voltage rises above $V_{SYSREG(LO)}$ (approximately 3.5V), the battery FET is turned on fully and the battery is charged with the full programmed charge current set by ISET. The charge current is regulated to I_{CHARGE} until the voltage between BAT and PGND reaches the regulation voltage. The voltage between BAT and PGND is regulated to V_{BATREG} (CV mode) while the charge current naturally tapers down as shown in Figure 10. During CV mode, the SYS output remains connected to the battery. The impedance of the battery FET is increased to 4x of the fully on value when IBAT falls below ~350mA to provide increased accuracy during termination. This will show a small rise in the SYS voltage when the $R_{DS(ON)}$ increases below ~350mA.

Once the charge current tapers down to the termination threshold, I_{TERM}, and the battery voltage is above the recharge threshold, the bq24266 terminates charge, turns off the battery charging FET and enters battery detection (see Battery Detection section for more details). The system output is regulated to the $V_{SYSREG(HI)}$ and supports the full current available from the input. The battery supplement mode is available to supply any SYS load that cannot be supported by the input source (see the *Dynamic Power Path Management* section for more details). The termination current level is set to 10% of the charge current. Termination is disabled when any loop is active other than CC or CV. This includes V_{INDPM}, input current limit, or thermal regulation. Termination is also disabled during TS warm/cool conditions.

A charge cycle is initiated when one of the following conditions is detected:

1. The battery voltage falls below the V_{BATREG}-V_{RCH} threshold.
2. IN Power-on reset (POR)
3. Charge disabled then enabled using $\overline{CE}$
4. IUSB toggeld from high impedance to any charge state

7.4.5 Charge Time Optimizer

The CC to CV transition is enhanced in the bq24266 architecture. The "knee" between CC and CV is very sharp. This enables the charger to remain in CC mode as long as possible before beginning to taper the charge current (CV mode). This provides a decrease in charge time as compared to older topologies.

7.4.6 Battery Detection

When termination conditions are met, a battery detection cycle is started. During battery detection, I_{DETECT} is pulled from V_{BAT} for $t_{DETECT(SNK)}$ to verify there is a battery. If the battery voltage remains above V_{DETECT} for the full duration of $t_{DETECT(SNK)}$, a battery is determined to present and the IC enters “Charge Done”. If V_{BAT} falls below V_{DETECT}, battery detection continues. The next cycle of battery detection, the bq24266 turns on $I_{BATSHRT}$ for $t_{DETECT(SRC)}$. If V_{BAT} rises to $V_{DET(SRC1)}$, the current source is turned off. In order to keep VBAT high enough to close the battery protector, the current source turns on if V_{BAT} falls to $V_{DET(SRC2)}$. The source cycle continues for $t_{DETECT(SRC)}$. After $t_{DETECT(SRC)}$, the battery detection continues through another current sink cycle. Battery detection continues until charge is disabled, the bq24266 enters high-z mode or a battery is detected. Once a battery is detected, a new charge cycle begins. With no battery connected, the BAT output will transition from V_{RCH} to PGND with a high period of $t_{DETECT(SRC)}$ and a low period of $t_{DETECT(SNK)}$. See Figure 16 in the *Application Curves* section.

7.4.7 Battery Overvoltage Protection (BOVP)

If the battery is ever above the battery OVP threshold (V_{BOVP}), the battery OVP circuit shuts the PWM converter off and the battery FET is turned on to discharge the battery to safe operating levels. In this condition, the V_{BATREG} is reset and may be below the battery voltage. This state can be entered when TS WARM conditions decrease the V_{BATREG} to less than the battery voltage. The battery OVP condition is cleared when the battery voltage falls below the hysteresis of V_{BOVP} by the battery discharging. When a battery OVP event exists for $t_{DGL(BOVP)}$, the bq24266 turns the battery FET and BGATE on.

7.4.8 Dynamic Power Path Management

The bq24266 features a SYS output that powers the external system load connected to the battery. This output is active whenever a valid source is connected to IN or BAT. When $V_{SYS} > V_{SYSREG(LO)}$, the SYS output is connected to V_{BAT}. If the battery voltage falls to V_{MINSYS}, V_{SYS} is regulated to the $V_{SYSREG(LO)}$ threshold to maintain the system output even with a deeply discharged or absent battery. In this mode, the SYS output voltage is regulated by the buck converter and the battery FET is linearly regulated to regulate the charge current

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Device Functional Modes (continued)

into the battery. The current from the supply is shared between charging the battery and powering the system load at SYS. The dynamic power path management (DPPM) circuitry of the bq24266 monitors the current limits continuously and if the SYS voltage falls to the V_{MINSYS} threshold, it adjusts charge current to maintain the minimum system voltage and supply the load on SYS. If the charge current is reduced to zero and the load increases further, the bq24266 enters battery supplement mode. During supplement mode, the battery FET is turned on and $V_{BAT} = V_{SYS}$ while the battery supplements the system load.

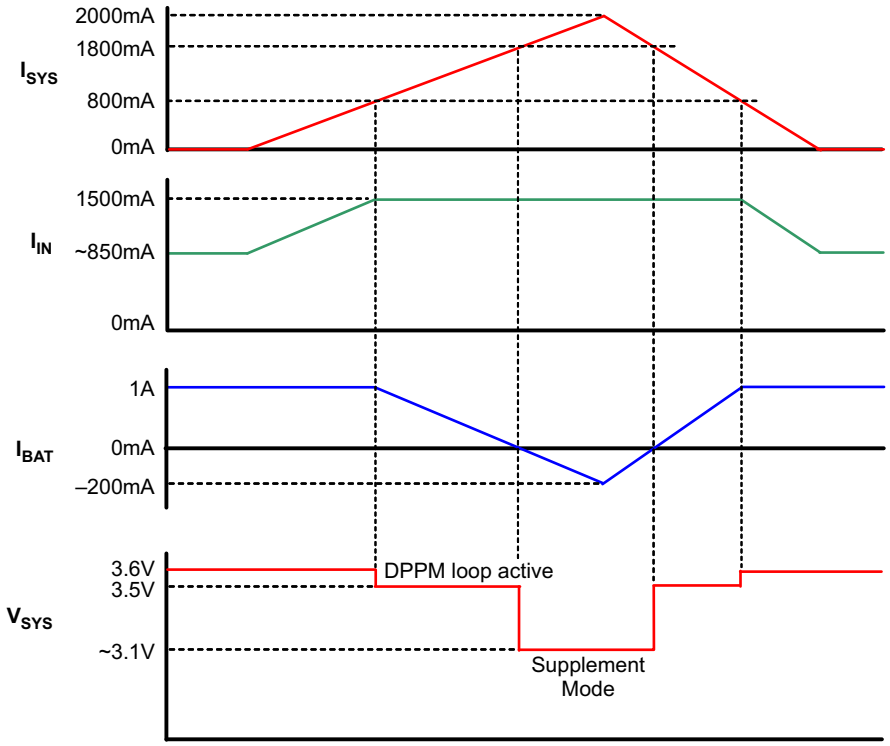


Figure 11. Example DPPM Response (V_{Supply} = 5V, V_{BAT} = 3.1V, 1.5A Input Current Limit)

7.4.9 Battery Discharge FET (BGATE)

The bq24266 contains a MOSFET driver to drive an external discharge FET between the battery and the system output. This external FET provides a low impedance path for supplying the system from the battery. Connect BGATE to the gate of the external discharge P-channel MOSFET. BGATE is on (low) under the following conditions:

1. No input supply connected.
2. IUSB1, IUSB2, IUSB3 pins = high

7.4.10 IUSB1, IUSB2, and IUSB3 Input

The bq24266 has three inputs that configure the input current limit and VINDPM thresholds. These input are also used to enable the USB OTG Boost function. The bq24266 incorporates all of the necessary input current limits to support USB2.0 and USB3.0 standards, as well as 1.5A to support wall adapters. Driving IUSB1, IUSB2, and IUSB3 all high places the bq24266 in Hi-Z mode where the buck converter is shutdown regardless if an input is connected to IN. Table 1 shows the configuration for IUSB1, IUSB2, and IUSB3.

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Device Functional Modes (continued)

Table 1. IUSB1, IUSB2, and IUSB3 Configurations

IUSB3	IUSB2	IUSB1	MODE	INPUT CURRENT LIMIT	VINDPM THRESHOLD
0	0	0	Charger	100mA	4.28V
0	0	1	Charger	500mA	4.44V
0	1	0	Charger	1.5A	External
0	1	1	Boost	---	---
1	0	0	Charger	150mA	4.28V
1	0	1	Charger	900mA	4.44V
1	1	0	Charger	2500mA	External
1	1	1	High Impedance	---	---

7.4.11 Safety Timer in Charge Mode

At the beginning of the charging process, the bq24266 starts the safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, the IC enters suspend mode where charging is disabled. $\overline{CE}$, or power must be toggled in order to clear the safety timer fault. The bq24266 also contains a 2X_TIMER that doubles the safety timer to prevent premature safety timer expiration when the charge current is reduced by a load on SYS or a NTC condition. When 2X_TIMER is active, the timer runs at half speed when any loop is active other than CC or CV. This includes V_{INDPM}, input current limit, or thermal regulation. The timer also runs at half speed during TS warm/cool conditions.

7.4.12 LDO Output (DRV)

The bq24266 contains a linear regulator (DRV) that is used to supply the internal MOSFET drivers and other circuitry. Additionally, DRV supplies up to 10mA external loads to power the $\overline{PG}$ or $\overline{CHG}$ LED or the USB transceiver circuitry. The maximum value of the DRV output is 5.3V so it ideal to protect voltage sensitive USB circuits. The LDO is on whenever a supply is connected to the input of the bq24266. The DRV is disabled under the following conditions:

1. V_{SUPPLY} < UVLO
2. V_{SUPPLY} < V_{BAT} + V_{SLP}
3. Thermal Shutdown

7.4.13 External NTC Monitoring (TS)

The bq24266 provides a flexible, voltage based TS input for monitoring the battery pack NTC thermistor. The bq24266 implements the full JEITA standard. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. The JEITA specification is shown in Figure 12.

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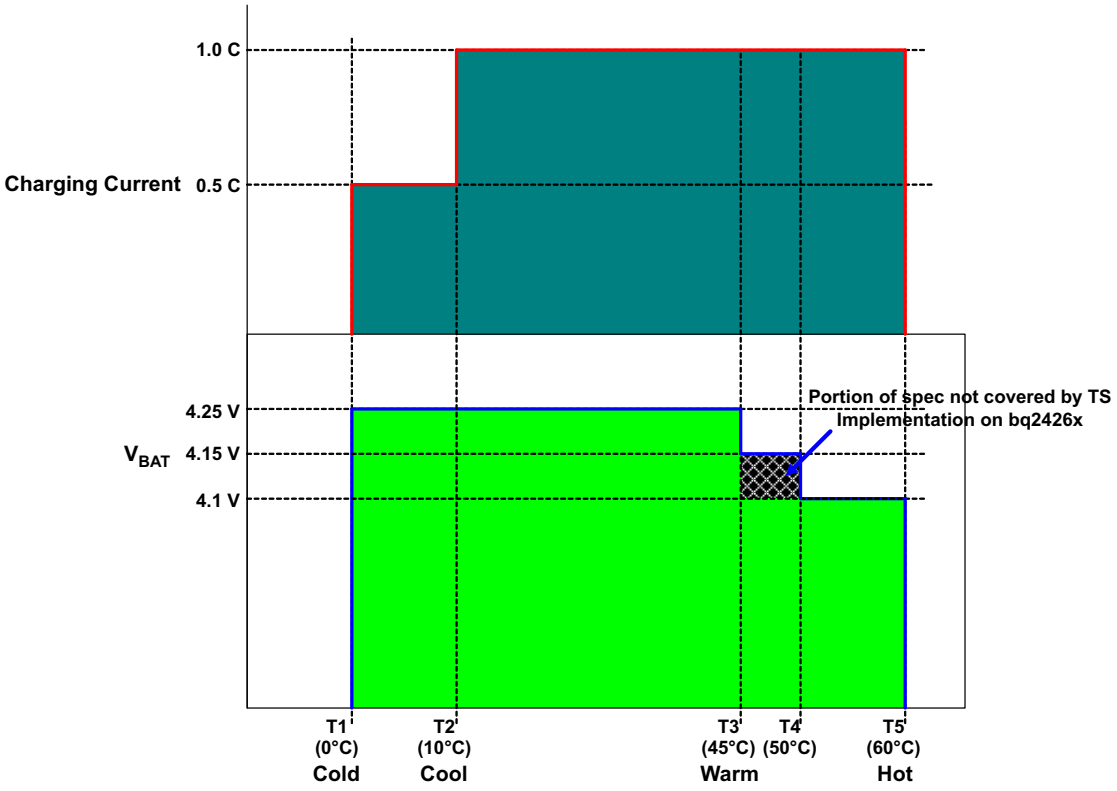


Figure 12. Charge Current During TS Conditions

To satisfy the JEITA requirements, four temperature thresholds are monitored; the cold battery threshold (T_{NTC} < 0°C), the cool battery threshold (0°C < T_{NTC} < 10°C), the warm battery threshold (45°C < T_{NTC} < 60°C) and the hot battery threshold (T_{NTC} > 60°C). These temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds in the EC table. Charging is suspended and timers are suspended when V_{TS} < V_{HOT} or V_{TS} > V_{COLD}. When V_{COOL} < V_{TS} < V_{COLD}, the charging current is reduced to half of the programmed charge current. When V_{HOT} < V_{TS} < V_{WARM}, the battery regulation voltage is reduced to 4.06V from the 4.2V regulation threshold. The TS function is disabled by connecting TS directly to DRV (V_{TS} > V_{TSOFF}).

The TS function is voltage based for maximum flexibility. Connect a resistor divider from DRV to GND with TS connected to the center tap to set the threshold. The connections are shown in Figure 13. The resistor values are calculated using the following equations:

$$RLO = \frac{V_{DRV} \times RCOLD \times RHOT \times \left[\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}}\right]}{RHOT \times \left[\frac{V_{DRV}}{V_{HOT}} - 1\right] - RCOLD \times \left[\frac{V_{DRV}}{V_{COLD}} - 1\right]} \quad (3)$$

$$RHI = \frac{\frac{V_{DRV}}{V_{COLD}} - 1}{\frac{1}{RLO} + \frac{1}{RCOLD}} \quad (4)$$

Where:

V_{COLD} = 0.60 × V_{DRV}

V_{HOT} = 0.30 × V_{DRV}

$$RCOOL = \frac{RLO \times RHI \times 0.564}{RLO - RLO \times 0.564 - RHI \times 0.564} \quad (5)$$

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$$RWARM = \frac{RLO \times RHI \times 0.383}{RLO - RLO \times 0.383 - RHI \times 0.383} \quad (6)$$

Where RHOT is the NTC resistance at the hot temperature and RCOLD is the NTC resistance at cold temperature.

The WARM and COOL thresholds are not independently programmable. The COOL and WARM NTC resistances for a selected resistor divider are calculated using Equation 5 and Equation 6.

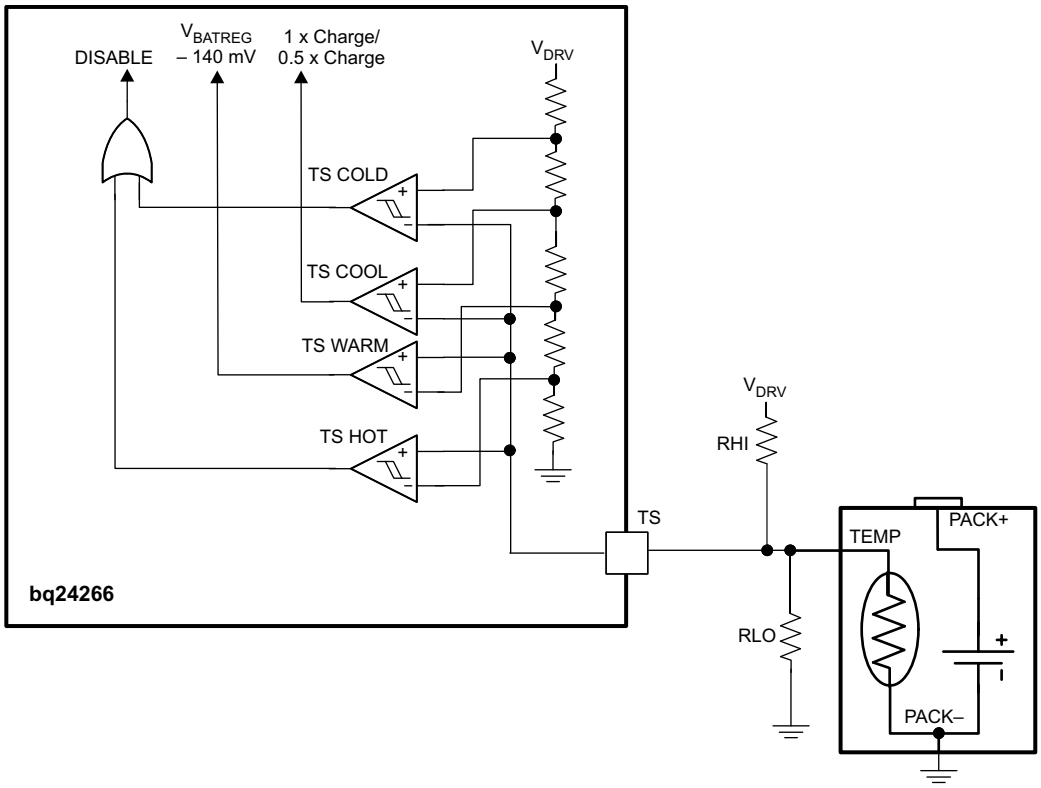


Figure 13. TS Circuit

7.4.14 Thermal Regulation and Protection

During the charging process, to prevent overheating in the chip, bq24266 monitors the junction temperature, T_J, of the die and reduces the input current once T_J reaches the thermal regulation threshold, T_{REG}. The input current is reduced to zero when the junction temperature increases about 10°C above T_{REG}. Once the input current is reduced to 0, the system current is reduced while the battery supplements the load to supply the system. When the input current is completely reduced to 0 and T_J>125°C, this is may cause a thermal shutdown of the bq24266 if the die temperature rises too high. At any state, if T_J exceeds T_{SHTDWN}, bq24266 stops charging and disables the buck converter. During thermal shutdown mode, PWM is turned off and all timers are suspended. The charge cycle resumes when T_J falls below T_{SHTDWN} by approximately 10°C.

7.4.15 Status Outputs ($\overline{CHG}$, $\overline{PG}$)

The $\overline{CHG}$ and $\overline{PG}$ outputs are used to indicate operating conditions for the bq24266. The $\overline{PG}$ output indicates that a valid input source is connected to V_{IN}. $\overline{PG}$ is low when (V_{BAT} + V_{SLP}) < V_{IN} < V_{OVP}. When there is no supply connected to the input within this range, $\overline{PG}$ is high impedance. Table 2 illustates the $\overline{PG}$ behavior under different conditions.

Table 2. $\overline{PG}$ Behavior

CHARGE STATE	$\overline{PG}$ BEHAVIOR
$V_{SUPPLY} < V_{UVLO}$	High Impedance
$V_{SUPPLY} < (V_{BAT} + V_{SLP})$	High Impedance
$(V_{BAT} + V_{SLP}) < V_{IN} < V_{OVP}$	Low
$V_{SUPPLY} > V_{OVP}$	High Impedance

The $\overline{CHG}$ output indicates new charge cycles. When a new charge cycle is initiated by $\overline{CE}$ or toggling the input power, $\overline{CHG}$ goes low and remains low until termination. After termination, $\overline{CHG}$ remains high impedance until a new charge cycle is initiated or the battery is removed/re-inserted. $\overline{CHG}$ does not go low during recharge cycles. Table 3 illustrates the $\overline{CHG}$ behavior under different conditions.

Connect $\overline{PG}$ and $\overline{CHG}$ to the DRV output through an LED for visual indication, or connect through a 100kΩ pullup to the required logic rail for host indication.

Table 3. $\overline{CHG}$ Behavior

CHARGE STATE	$\overline{CHG}$ BEHAVIOR
Charge in Progress	Low (first charge cycle) High-Impedance (recharge cycles)
Charge suspended by /CE or TS function	
Charging Suspended by Thermal Loop	
Charging Done	High-Impedance
Recharge Cycle after Termination	
Timer Fault	
No Valid Supply $V_{IN} > V_{OVP}$ or VIN < $(V_{BAT} + V_{SLP})$	
No Battery Present	

7.4.16 Boost Mode Operation

When the IUSB inputs are configured in Boost Mode (IUSB3 = 0, IUSB2 = IUSB1 = 1), the device operates in boost mode and delivers 5V to IN to supply USB OTG devices connected to the USB connector.

7.4.16.1 PWM Controller in Boost Mode

Similar to charge mode operation, in boost mode the IC switches at 1.5MHz to regulate the voltage at IN to 5V. The voltage control loop is internally compensated to provide enough phase margin for stable operation with the the battery from 3.3V to 4.2V up to 1A.

In boost mode, the cycle-by-cycle current limit is set to 4A to provide protection against short circuit conditions. If the cycle-by-cycle current limit is active for 8ms, an overload condition is detected and the device exits boost mode, and signals an over-current fault. Additionally, discharge current limit ($I_{LIM(DISCHG)}$) is active to protect the battery from overload. Synchronous operation and burst mode are used to maximize efficiency over the full load range.

The bq24266 will not enter boost mode unless the IN voltage is less than the UVLO. When the boost function is enabled, the bq24266 enters a linear mode to bring IN up to the battery voltage. Once $V_{IN} > (V_{BAT} – 1V)$, the bq24266 begins switching and regulates IN up to 5V. If V_{IN} does not rise to within 1V of V_{BAT} within 8ms, an over-current event is detected and boost mode is exited.

7.4.16.2 Burst Mode during Light Load

In boost mode, the IC operates using burst mode to improve light load efficiency and reduce power loss. During boost mode, the PWM converter is turned off when the device reaches minimum duty cycle and the output voltage rises to $V_{BURST(ENT)}$ threshold. This corresponds to approximately a 75mA inductor current. The converter then restarts when V_{IN} falls to $V_{BURST(EXT)}$. See Figure 22 in the Typical Operating Characteristics for an example waveform.

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7.4.16.3 $\overline{CHG}$ and $\overline{PG}$ During Boost Mode

During boost mode, the $\overline{CHG}$ and $\overline{PG}$ outputs are high impedance.

7.4.16.4 Protection in Boost Mode

7.4.16.4.1 Output Over-Voltage Protection

The bq24266 contains integrated over-voltage protection on the IN pin. During boost mode, if an over-voltage condition is detected ($V_{IN} > V_{BOOSTOVP}$), after deglitch $t_{DGL(BOOST_OVP)}$, the IC turns off the PWM converter unitl the IUSB pins are toggled. The converter does not restart when V_{IN} drops to the normal level until the IUSB pins are toggled.

7.4.16.4.2 Output Over-Current Protection

The bq24266 contains over current protection to prevent the device and battery damage when IN is overloaded. When an over-current condition occurs, the cycle-by-cycle current limit limits the current from the battery to the load. If the overload condition lasts for 8ms, the overload fault is detected. When an overload condition is detected, the bq24266 turns off the PWM converter. The boost operation starts only after the fault is cleared and the IUSB pins are toggled.

7.4.16.4.3 Battery Voltage Protection

During boost mode, when the battery voltage is below the minimum battery voltage threshold, $V_{BATUVLO}$, the IC turns off the PWM converter. Once the battery voltage returns to the acceptable level, the boost starts only after the IUSB pins are toggled. Proper operation below 3.3V down to the $V_{BATUVLO}$is not specified.

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8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq24266EVM-609 evaluation module (EVM) is a complete charger module for evaluating the bq24266. The application curves were taken using the bq24266EVM-609 (SLUUB40). See *Related Documentation* .

The bq24266EVM is shipped with the bq24266 populated, For the bq24266, the TS input is available and the resistors are chosen using Equation 3 and Equation 4.

8.2 Typical Applications

8.2.1 Typical Application, External Discharge FET

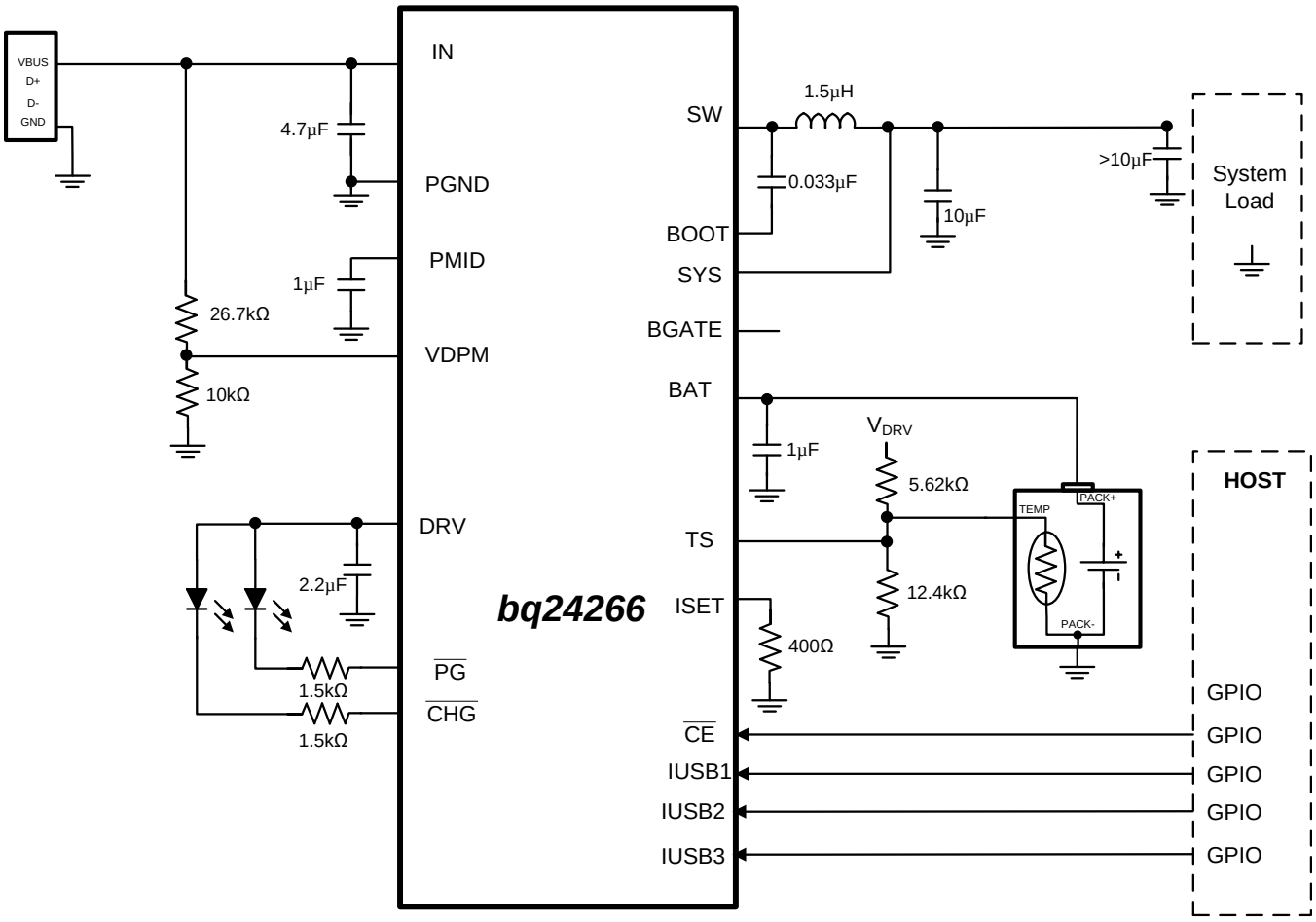


Figure 14. bq24266 Typical Application Circuit

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Typical Applications (continued)

8.2.1.1 Design Requirements

Table 4. Design Requirements

DESIGN PARAMATER	EXAMPLE VALUE
Input Voltage Range	4.75 V to 5.25 V nominal, withstand 28 V
Input Current Limit	2500 mA
Input DPM Threshold	4.2 V (Externally Set)
Fast Charge Current	3000 mA
Battery Charge Voltage	4.2 V
Termination Current	300 mA

8.2.1.2 Detailed Design Procedure

The parameters are configurable using the EVM jumper options as described in the Users Manual. The typical application for the bq24266EVM is shown in Figure 14. The default IUSB settings are for 2.5A input current limit and external V_{IN}DPM threshold, which is IUSB3 = 1, IUSB = 2 = 1, IUSB1 = 0. The VDPM resistors were selected using Equation 1. The charge current, I_{CHARGE}, was set to be 3A using Equation 2.

The typical application circuit shows the minimum capacitance requirements for each pin. Options for sizing the inductor outside the 1.5 µH recommended value and additional SYS pin capacitance are explained in the next section. The resistors on PG and CHG are sized per each LED's current requirements. The TS resistor divider for configuring the TS function to work with the battery's specific thermistor can be computed from Equation 3 and Equation 4. The external battery FET is optional.

8.2.1.2.1 Output Inductor and Capacitor Selection Guidelines

When selecting an inductor, several attributes must be examined to find the right part for the application. First, the inductance value should be selected. The bq24266 is designed to work with 1.5µH to 2.2µH inductors. The chosen value will have an effect on efficiency and package size. Due to the smaller current ripple, some efficiency gain is reached using the 2.2µH inductor, however, due to the physical size of the inductor, this may not be a viable option. The 1.5µH inductor provides a good tradeoff between size and efficiency.

Once the inductance has been selected, the peak current must be calculated in order to choose the current rating of the inductor. Use Equation 7 to calculate the peak current.

$$I_{PEAK} = I_{LOAD(MAX)} \times \left(1 + \frac{\%_{RIPPPLE}}{2}\right) \quad (7)$$

The inductor selected must have a saturation current rating greater than or equal to the calculated I_{PEAK}. Due to the high currents possible with the bq24266, a thermal analysis must also be done for the inductor. Many inductors have 40°C temperature rise rating. This is the DC current that will cause a 40°C temperature rise above the ambient temperature in the inductor. For this analysis, the typical load current may be used adjusted for the duty cycle of the load transients. For example, if the application requires a 1.5A DC load with peaks at 2.5A 20% of the time, a Δ40°C temperature rise current must be greater than 1.7A:

$$I_{TEMPRISE} = I_{LOAD} + D \times (I_{PEAK} - I_{LOAD}) = 1.5\ A + 0.2 \times (2.5\ A - 1.5\ A) = 1.7\ A \quad (8)$$

The internal loop compensation of the bq24266 is designed to be stable with 10µF to 150µF of local capacitance but requires at least 20µF total capacitance on the SYS rail (10µF local + ≥ 10µF distributed). The capacitance on the SYS rail can be higher than 150µF if distributed amongst the rail. To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 10µF and 47µF is recommended for local bypass to SYS. If greater than 100µF effective capacitance is on the SYS rail, place at least 10µF bypass on the BAT pin. Pay special attention to the DC bias characteristics of ceramic capacitors. For small case sizes, the capacitance can be derated as high as 70% at workable voltages. All capacitances specified in this datasheet are effective capacitance, not capacitor value.

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8.2.2 Application Curves

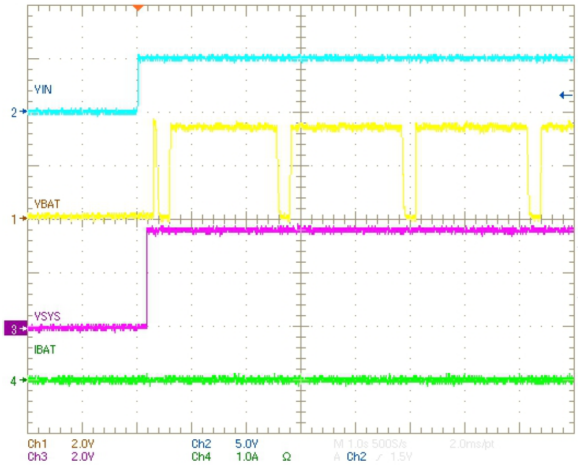


Figure 15. Startup With No Battery

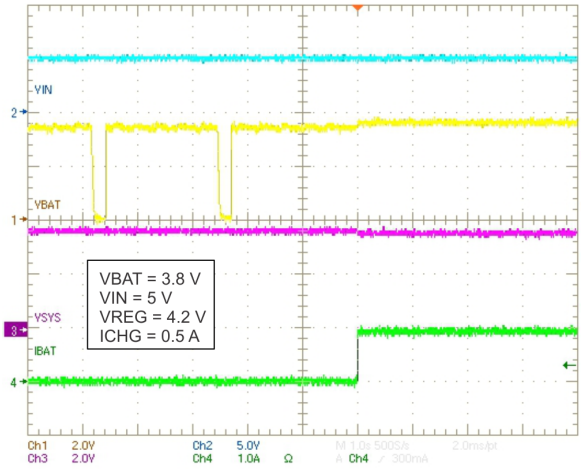


Figure 16. Battery Detection

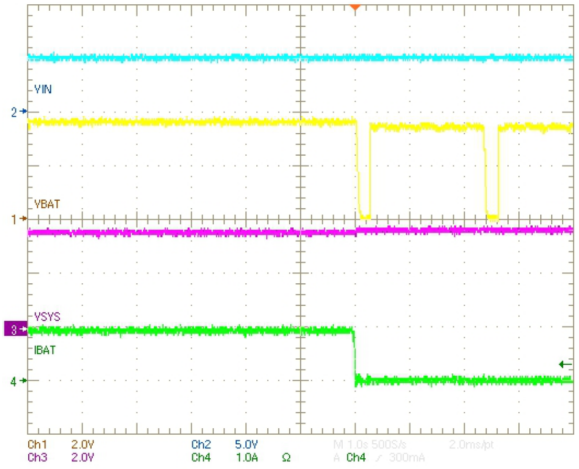


Figure 17. Battery Removal

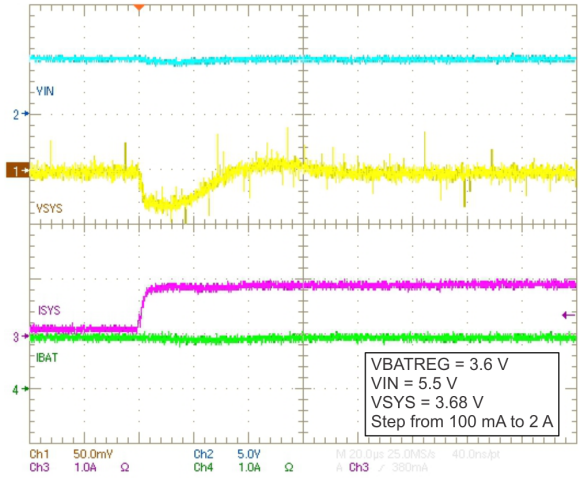


Figure 18. VSYS Transient Without Supplement Mode

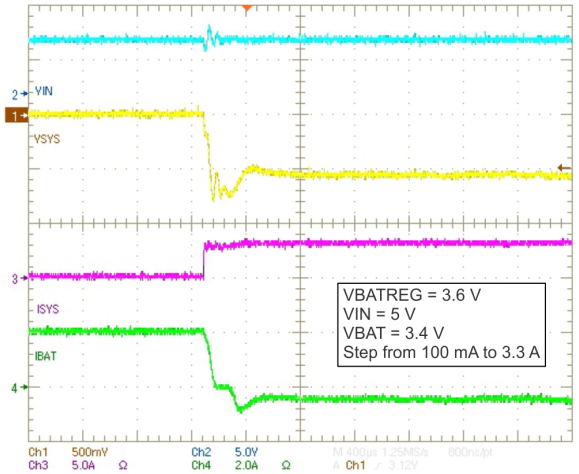


Figure 19. VSYS Transient With Supplement Mode

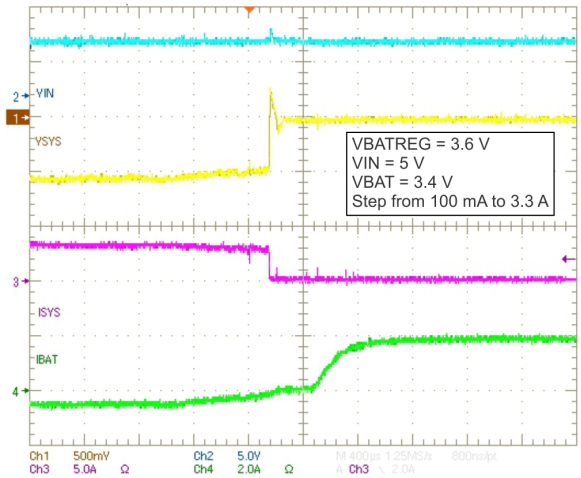


Figure 20. VSYS Transient With Supplement Mode

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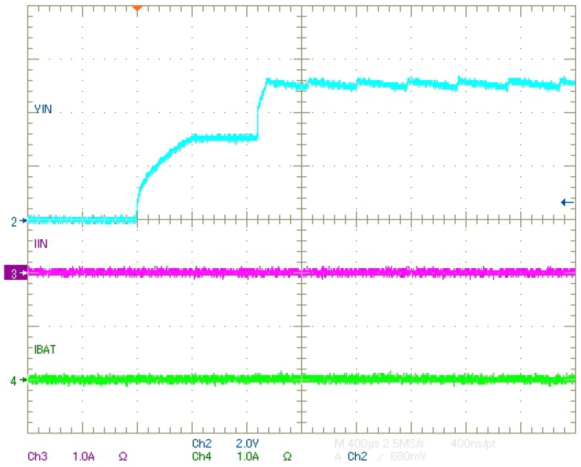


Figure 21. Boost Startup No Load

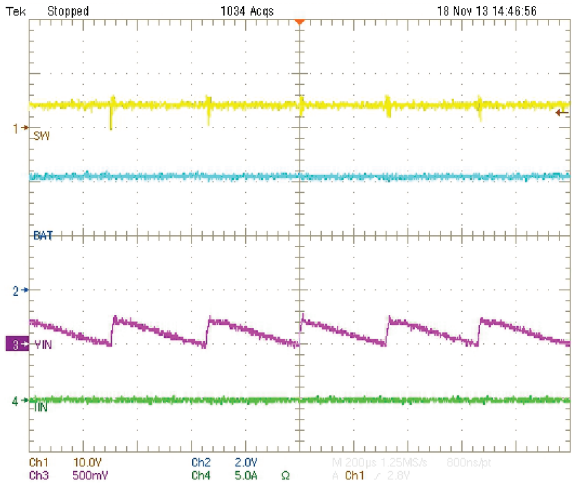


Figure 22. Boost Burst Mode During Light Load

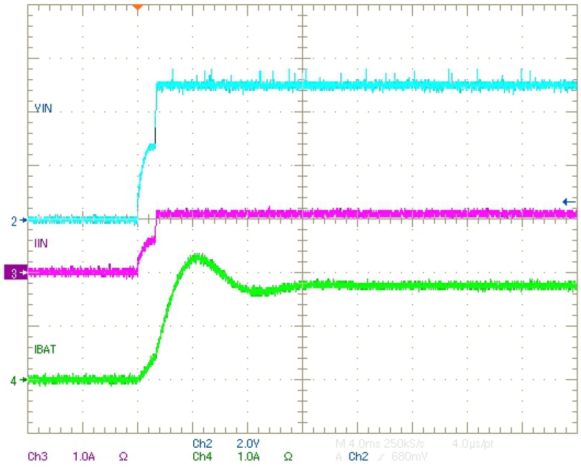


Figure 23. Boost Startup 1A Load

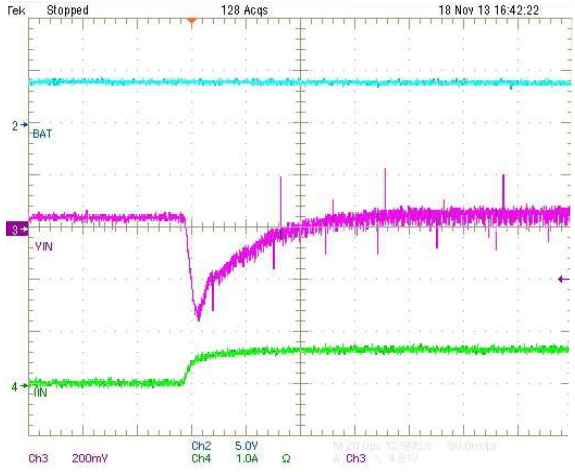


Figure 24. Boost Transient Response

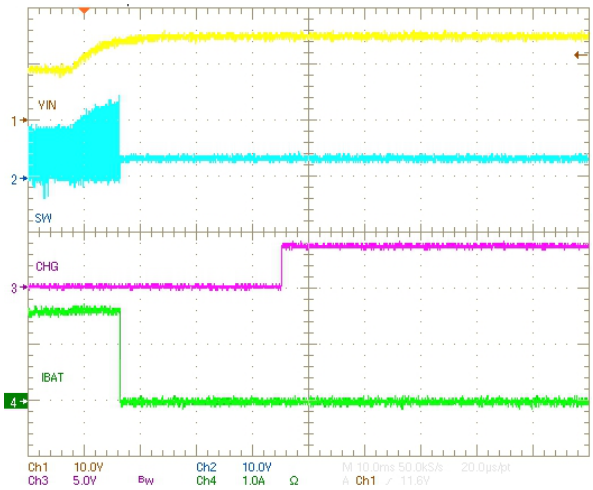


Figure 25. Input OVP Event with $\overline{\text{CHG}}$

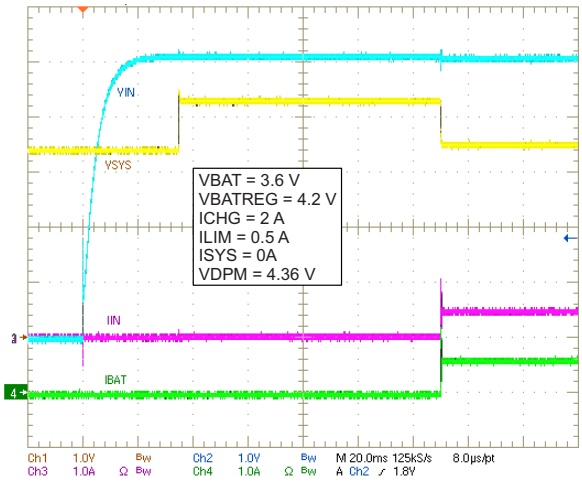
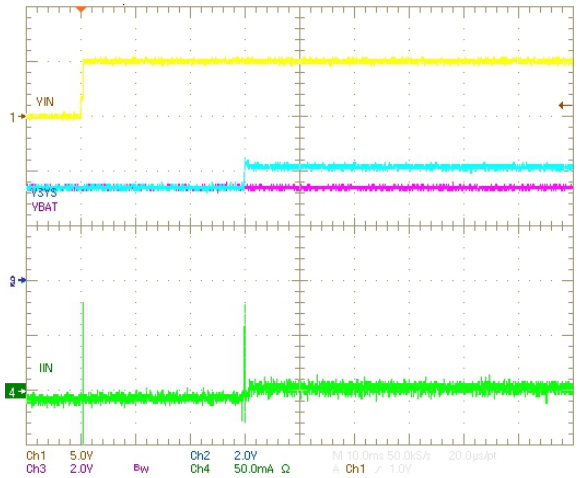
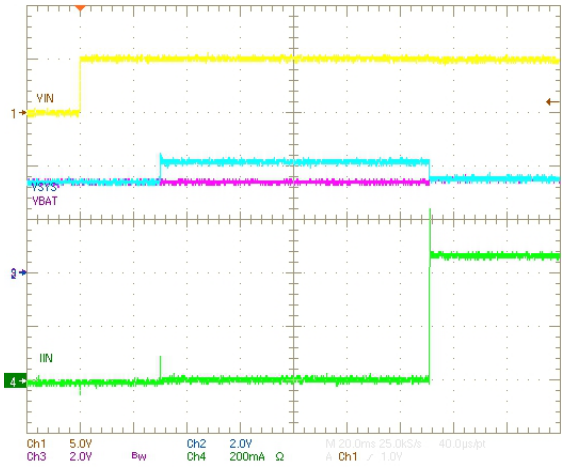


Figure 26. Startup, 4.2V



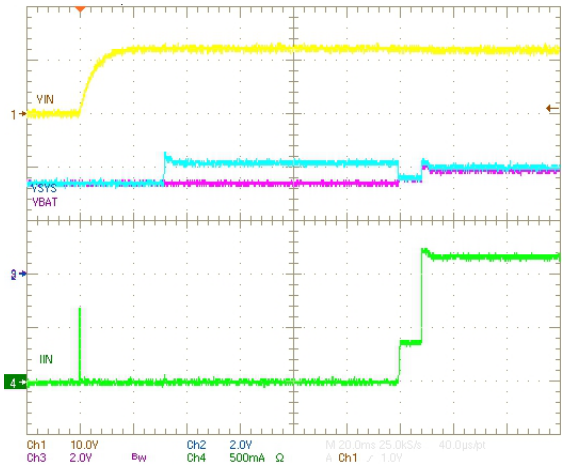
V_{IN} = 5 V

Figure 27. USB Inrush Current, IUSB3 = 0, IUSB2 = 0, IUSB1 = 1



V_{IN} = 5 V

Figure 28. Default Startup, IUSB3 = 0, IUSB2 = 0, IUSB1 = 1



V_{IN} = 12 V

Figure 29. Default Startup, IUSB3 = 1, IUSB2 = 1, IUSB1 = 0

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9 Power Supply Recommendations

9.1 Requirements for SYS Output

In order to provide an output voltage on SYS, the bq24266 requires either a power supply between 4.2 and 14 V with at least 100 mA current rating connected to IN; or, a single-cell Li-Ion battery with voltage > VBATUVLO connected to BAT. The source current rating needs to be at least 2.5 A in order for the buck converter of the charger to provide maximum output power to SYS.

9.2 Requirements for Charging

In order for charging to occur the source voltage measured at the IN pins of the IC, factoring in cable/trace losses from the source, must be greater than the VINDPM threshold, but less than the maximum values shown above. The current rating of the source must be higher than the buck converter needs to provide the load on SYS. For charging at a desired charge current of I_{CHRG}, V_{IN} x I_{IN} x η > V_{SYS} x ($_{ISYS}$+ I_{CHRG}) where η is the efficiency estimate from Figure 2 or Figure 3 and VSYS = VBAT when VBAT charges above VMINSYS. The charger limits I_{IN} to the current limit setting of that input. With ISYS = 0 A, the charger consumes maximum power at the end of CC mode, when the voltage at the BAT pin is near VBATREG but ICHRG has not started to taper off toward ITERM.

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10 Layout

10.1 Layout Guidelines

The following provides some guidelines:

- Place 1µF input capacitor as close to PMID pin and PGND pin as possible to make high frequency current loop area as small as possible.
- Connect the GND of the PMID and IN caps as close as possible.
- Place 4.7µF input capacitor as close to IN pin and PGND pin as possible to make high frequency current loop area as small as possible.
- The local bypass capacitor from SYS to GND should be connected between the SYS pin and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin.
- Place all decoupling capacitors close to their respective IC pin and as close as to PGND as possible. Do not place components such that routing interrupts power stage currents. All small control signals should be routed away from the high current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias. Two vias per capacitor for power-stage capacitors and one via per capacitor for small-signal components. It is also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results.
- The high-current charge paths into IN, BAT, SYS and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET.
- For high-current applications, the balls for the power paths should be connected to as much copper in the board as possible. This allows better thermal performance as the board pulls heat away from the IC.

10.2 Layout Example

It is important to pay special attention to the PCB layout. Figure 30 provides a sample layout for the high current paths of the bq24266RGE.

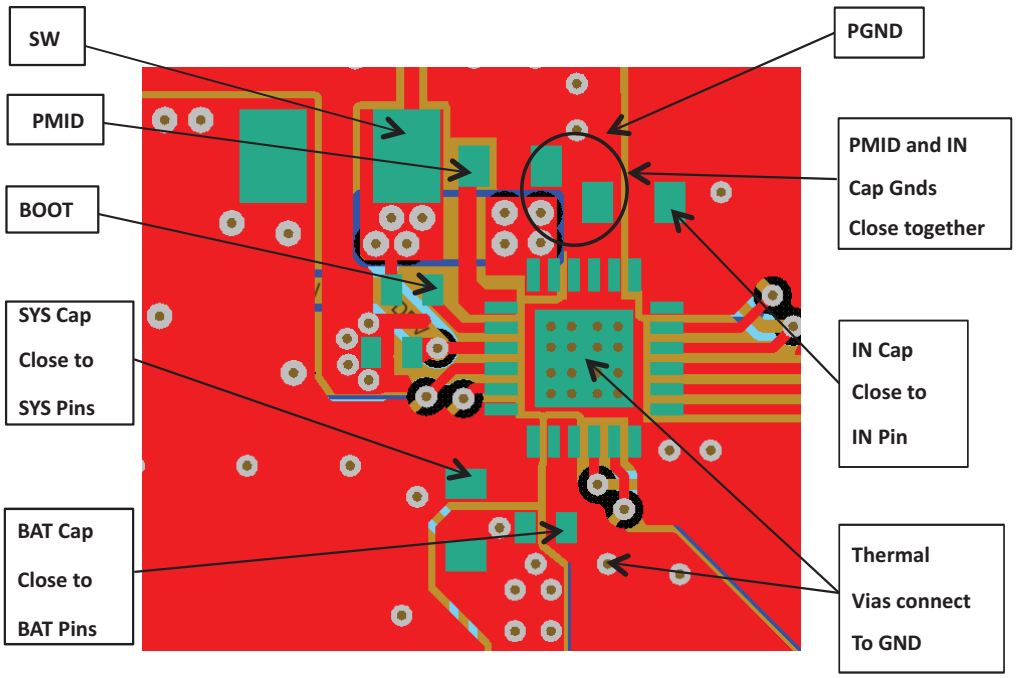


Figure 30. Recommended bq24266 PCB Layout for QFN Package

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

User's Guide for QFN Packaged bq24265, bq24266, and bq24267 3-A Battery Charger Evaluation Module, SLUUB40

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24266RGER	LIFEBUY	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24266	
BQ24266RGET	LIFEBUY	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24266	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

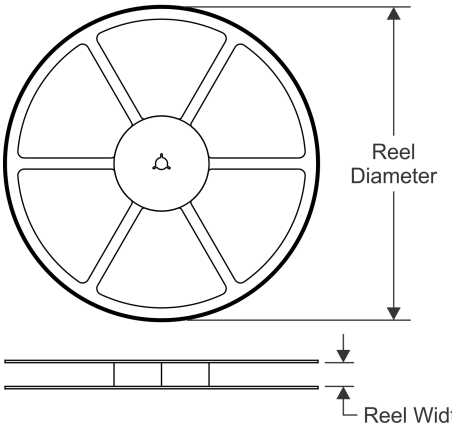
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

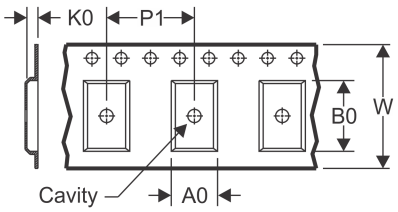
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

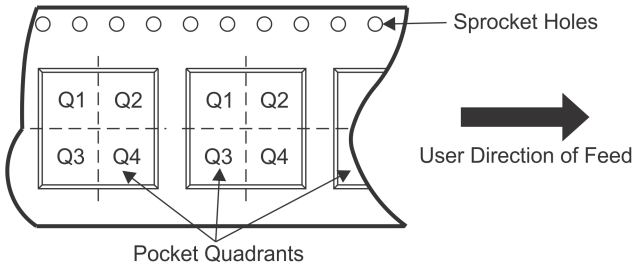


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

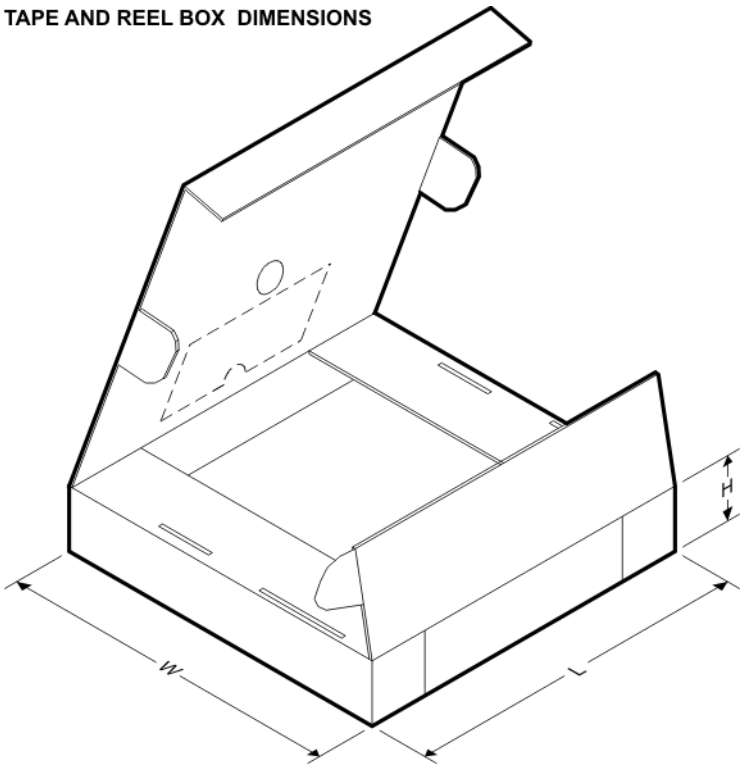
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24266RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24266RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



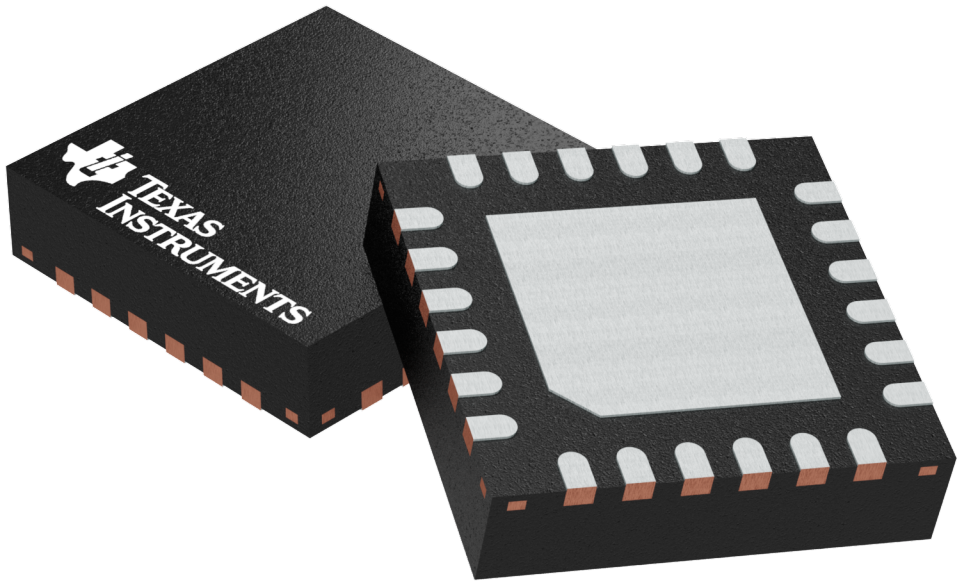
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24266RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24266RGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

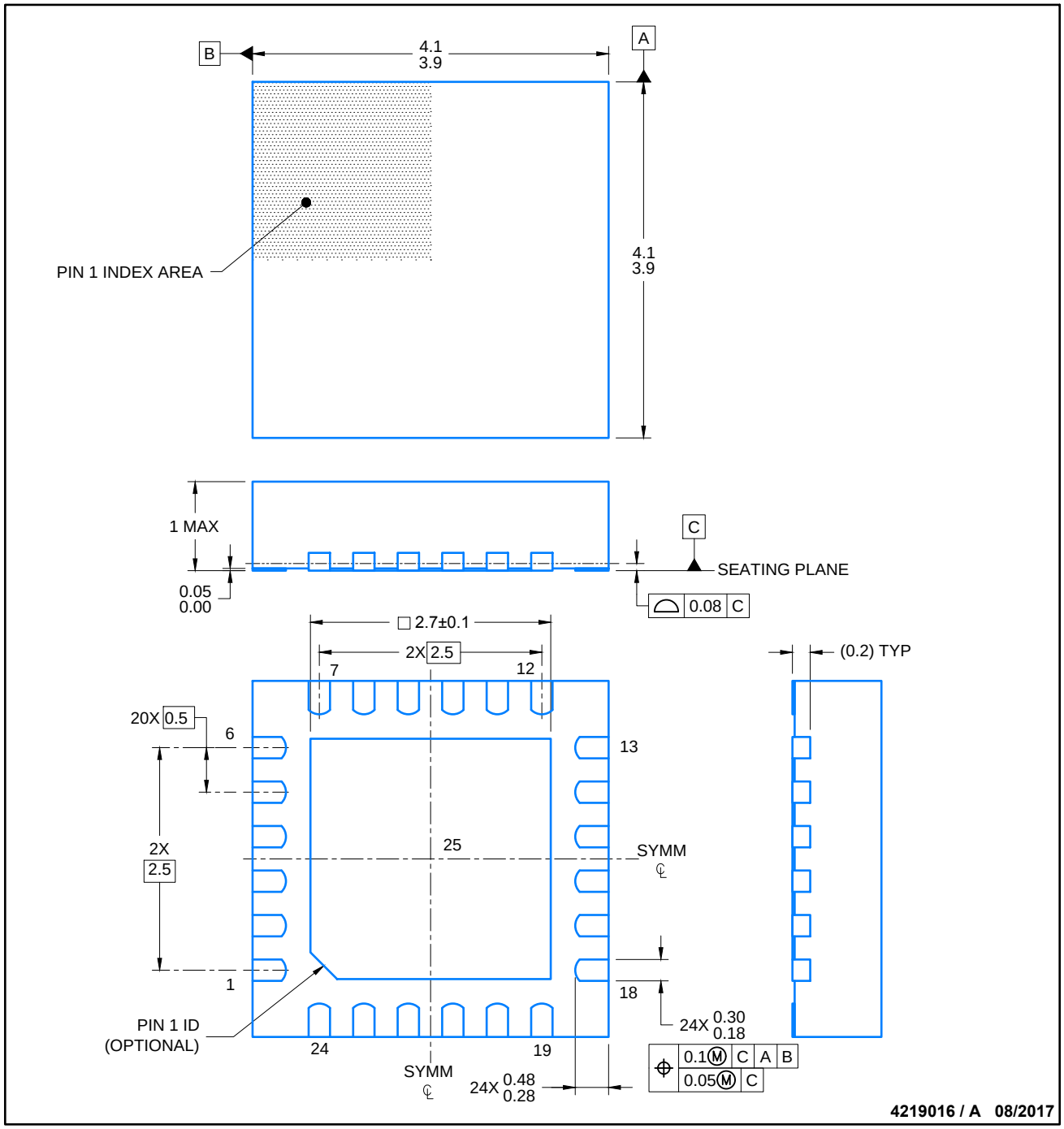
4204104/H

PACKAGE OUTLINE

RGE0024H

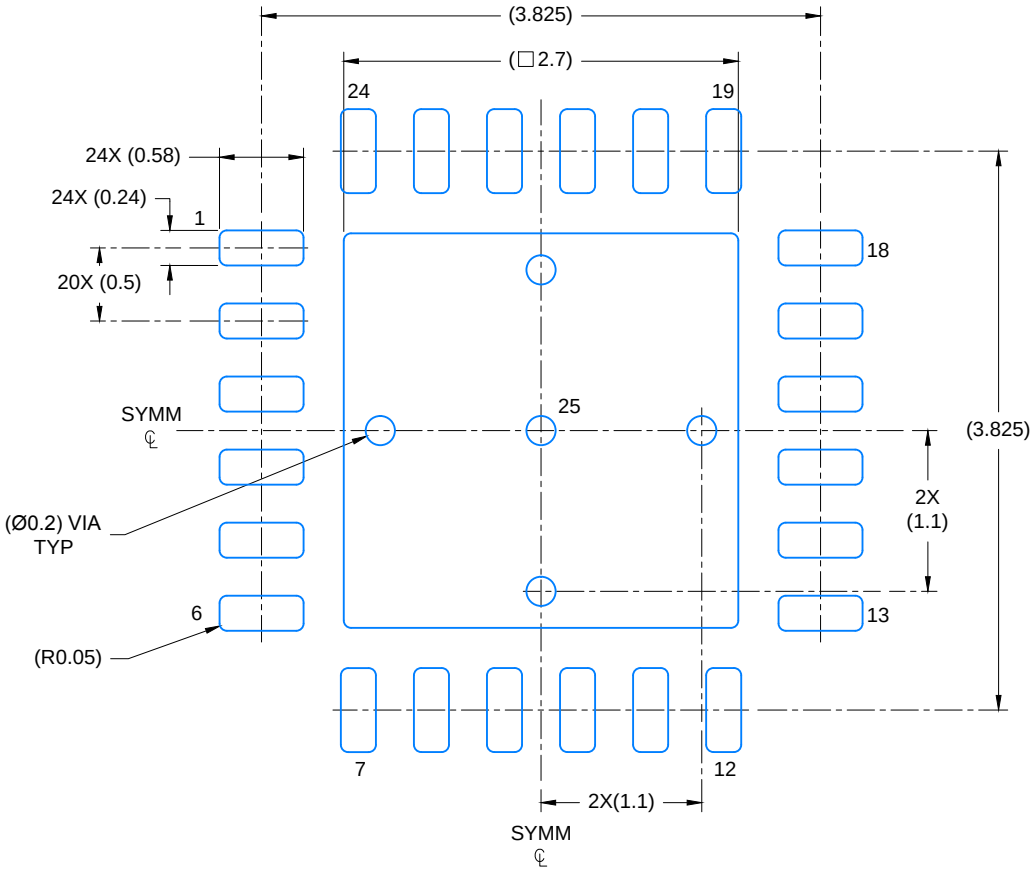
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



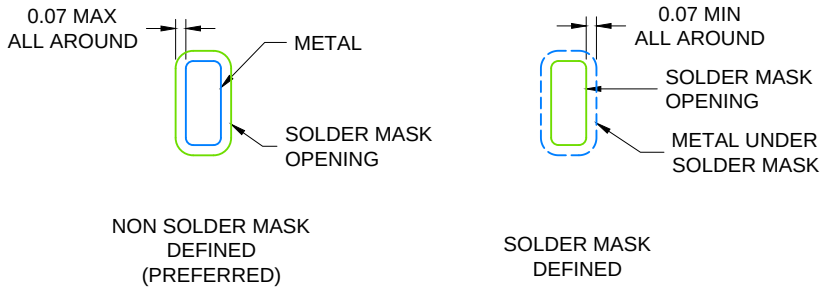
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

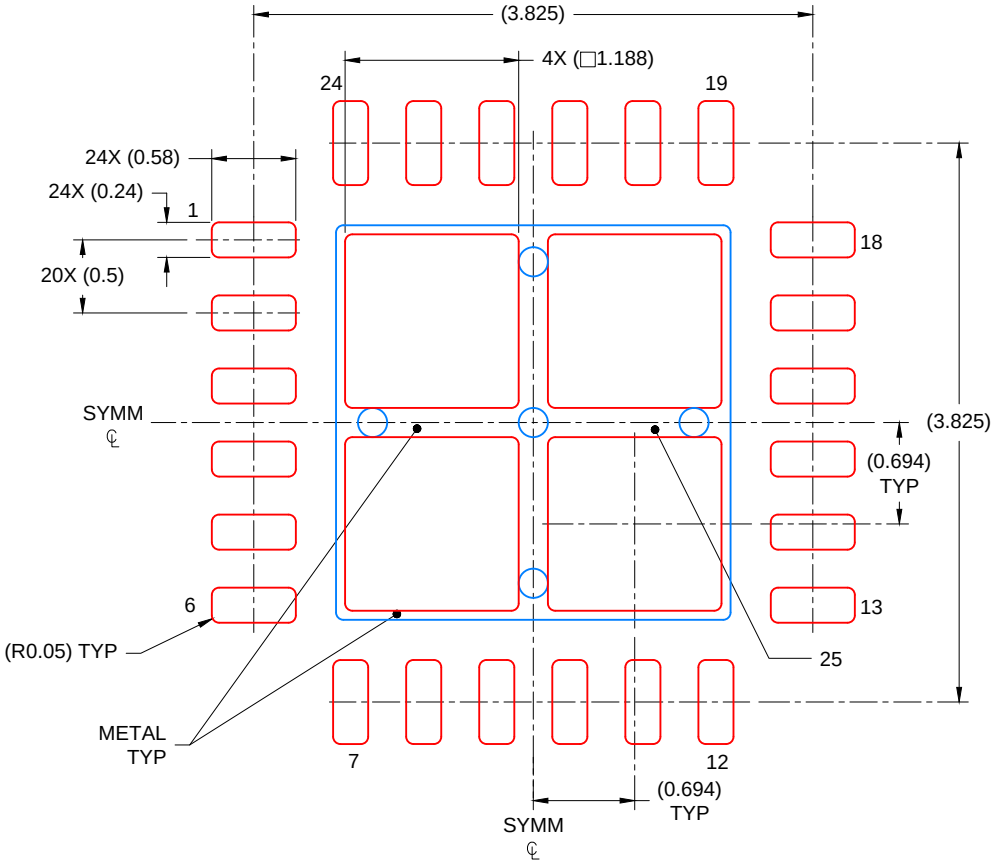


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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